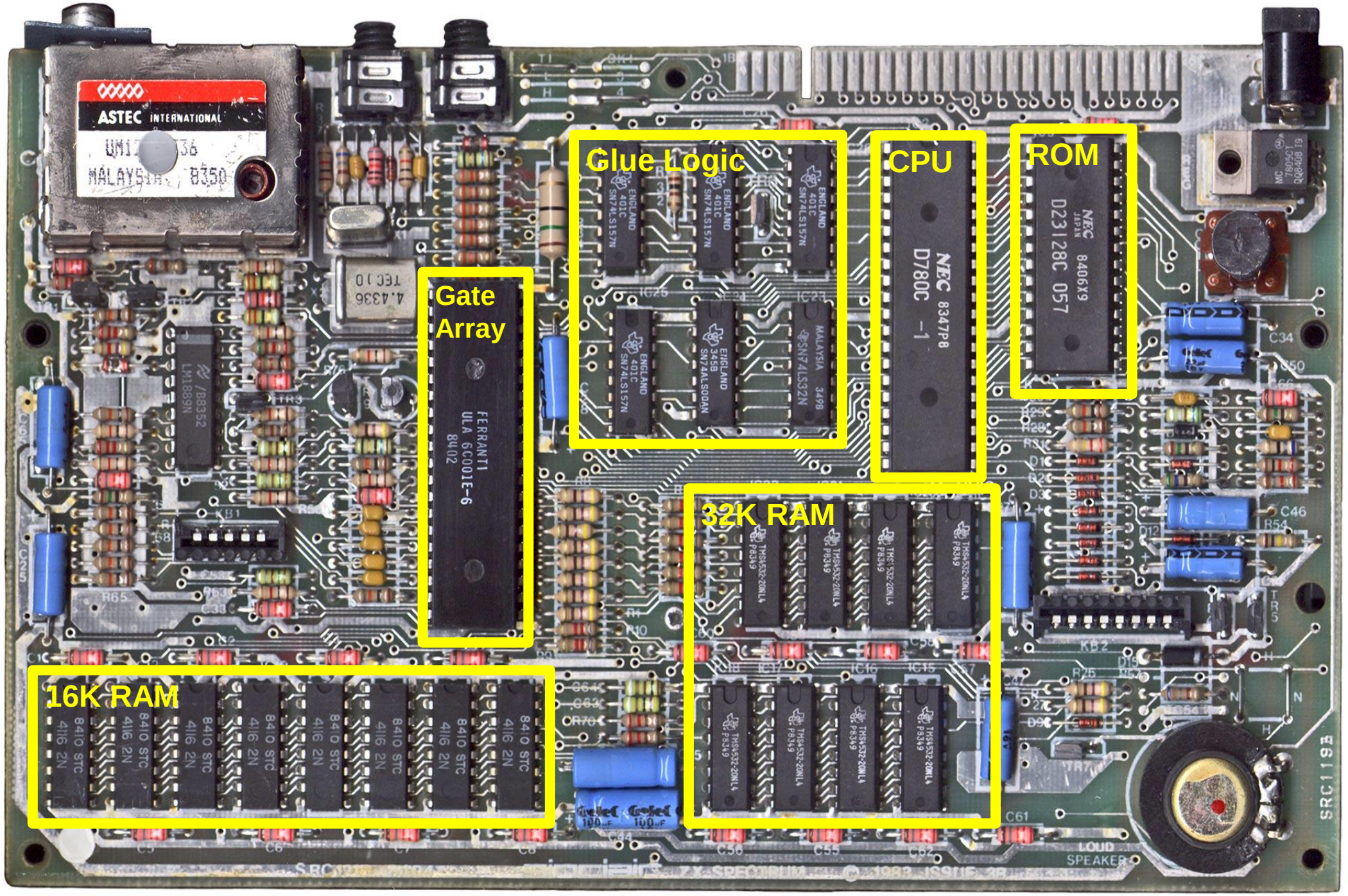
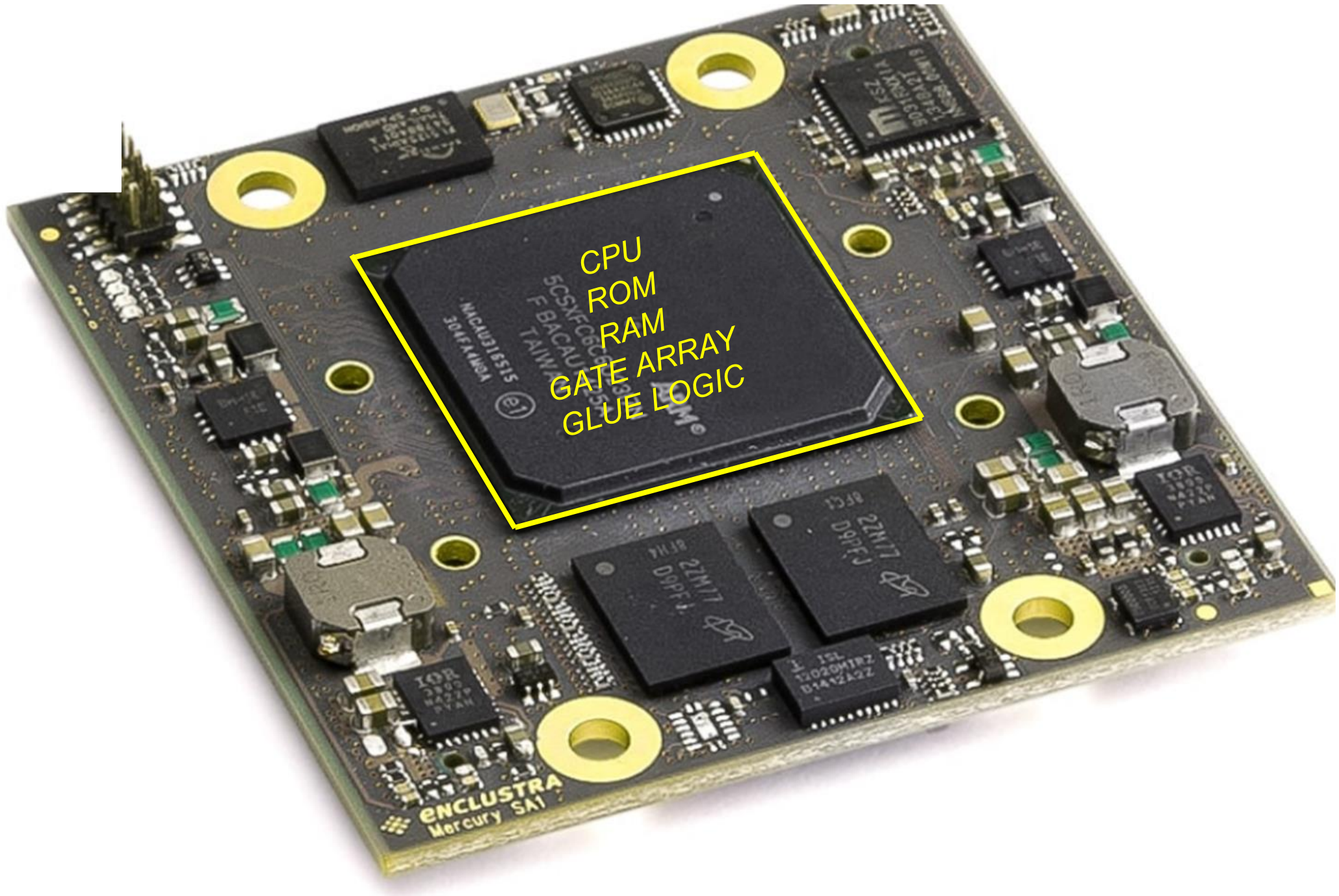
It’s a Hardware bug - and I can prove it

Kris Chaplin

Embedded Technology Specialist
Intel Programmable Solutions Group




CPU
ROM
RAM
GATE ARRAY
GLUE LOGIC
ENCLUSTRA
Mercury SA1


C:\

What is the problem?

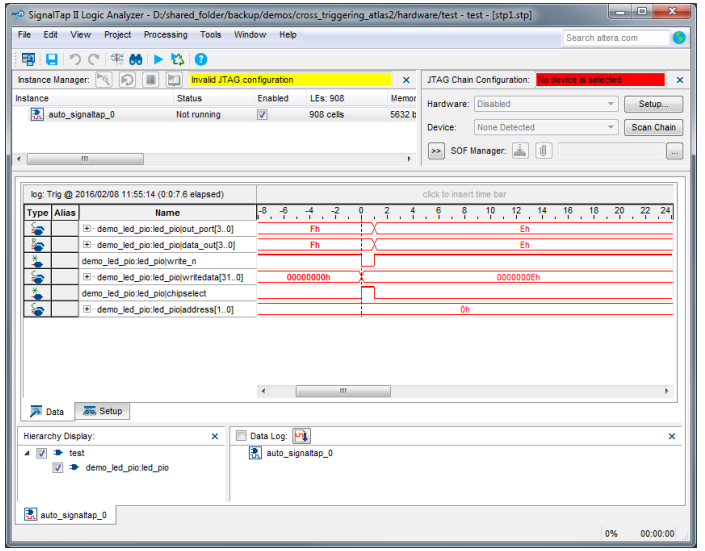
- Systems are getting more complex
- We are doing more in one chip
- Debug between hardware and software can be challenging
  - The hardware can keep changing as development continues
  - Hardware may not be fully tested when software is written
  - How do we narrow down the scope of the problem?
  - Is it a hardware or software bug? (or both?)

Why is it hardware / software co-debug important?

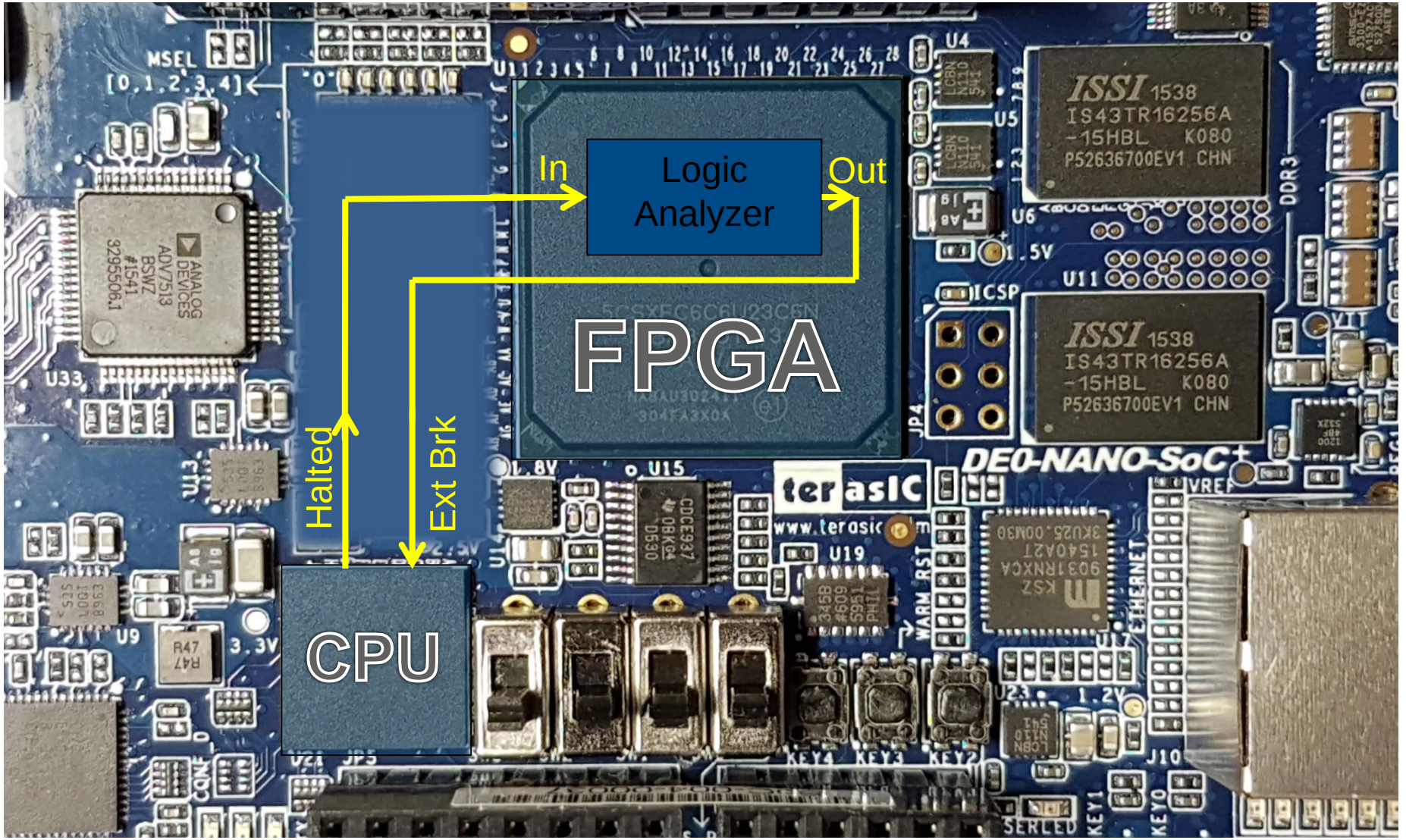
- Chasing bugs can be time consuming and soul destroying
  - Time can cause missed deadlines
  - Can even kill a project
- Device Errata or custom built hardware can result in unexpected bugs.
- The right tools and methodology can shave off significant time in resolving issues.

Low level debug tools

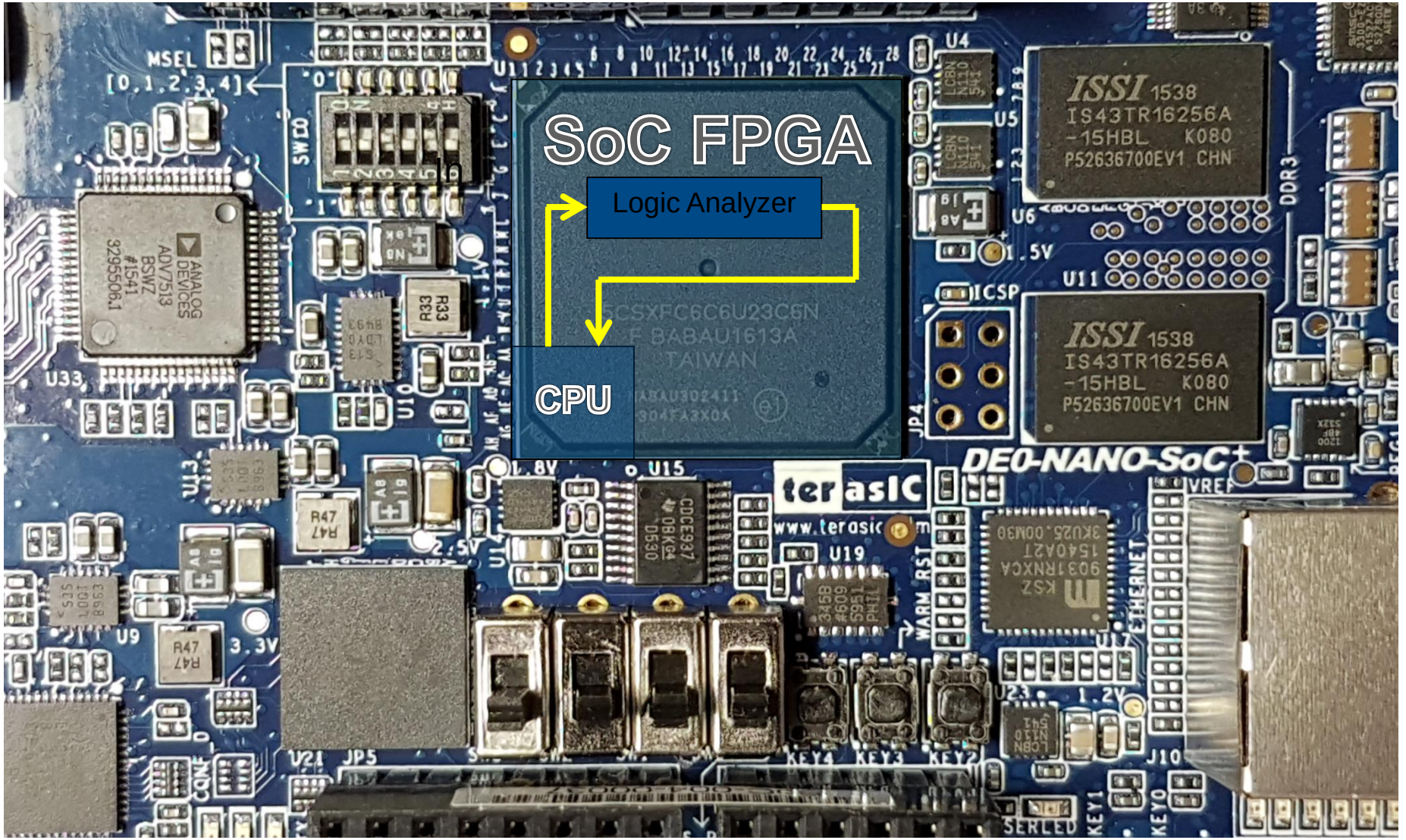
- Software: Many processors have JTAG debugging ports for fine grain single-stepping debug
  - Third party debug pods
    - ARM, Lauterbach, Olimex, Altera/Intel + many others
- Hardware: All modern programmable logic support JTAG Internal logic analyzers
  - Altera - Signal Tap
  - Xilinx - Chipscope Pro
  - Lattice - Reveal
    etc.



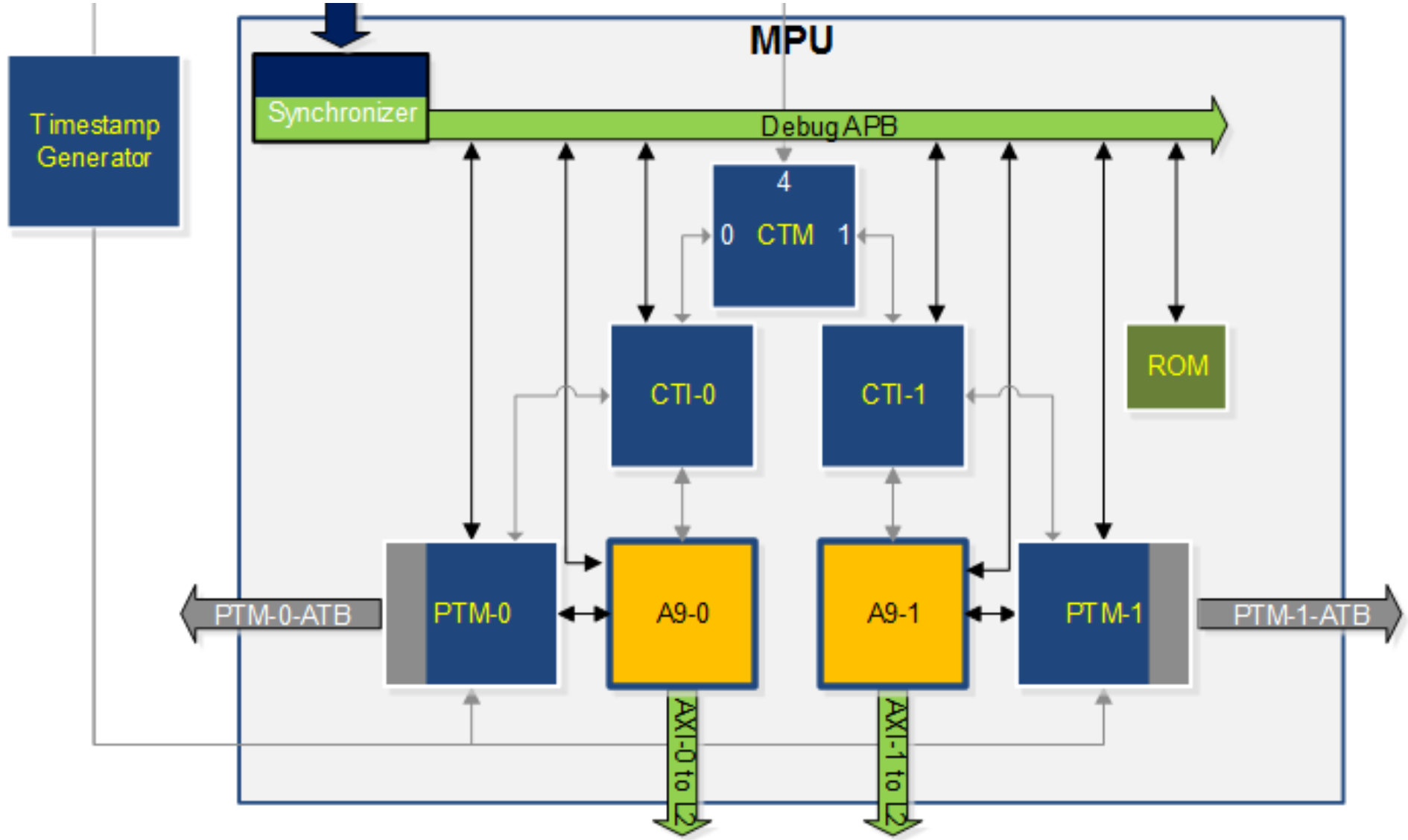
Software / Hardware Co-debug - the mechanics



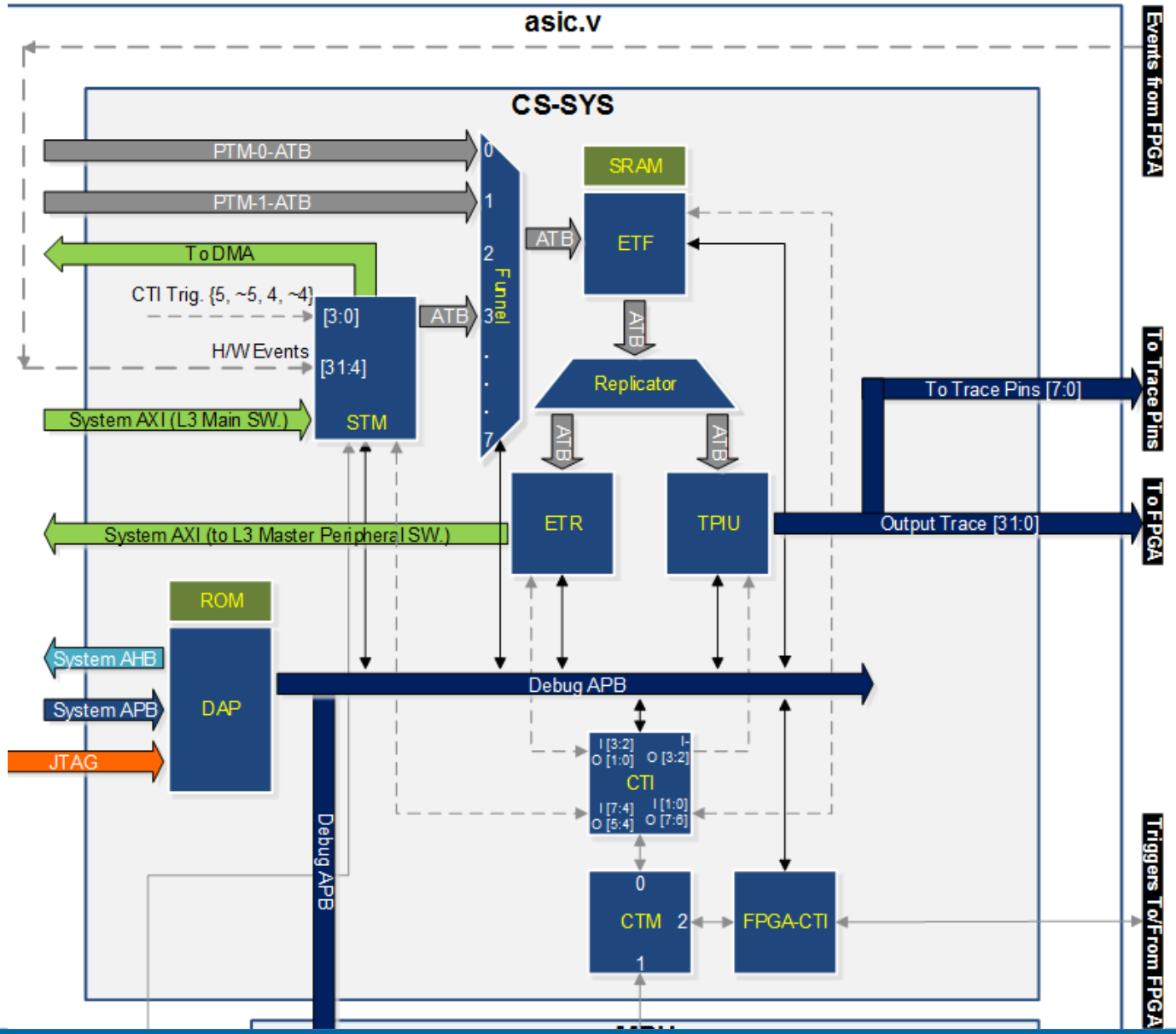
Software / Hardware Co-debug - the mechanics



Sample ARM Cross Triggering infrastructure

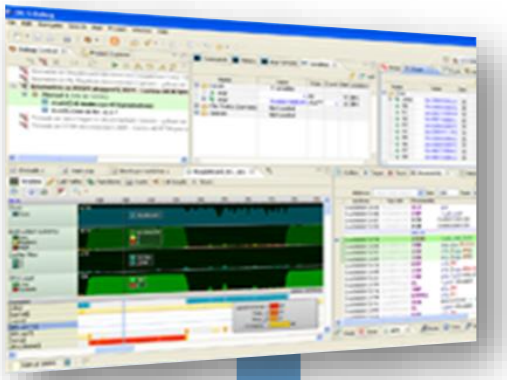


FPGA Cross Trigger Extensions



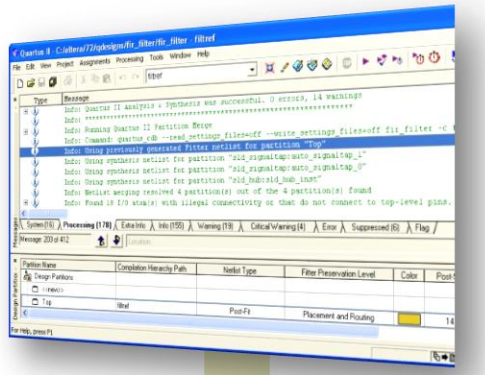
How does it fit together?

Software JTAG Debugger

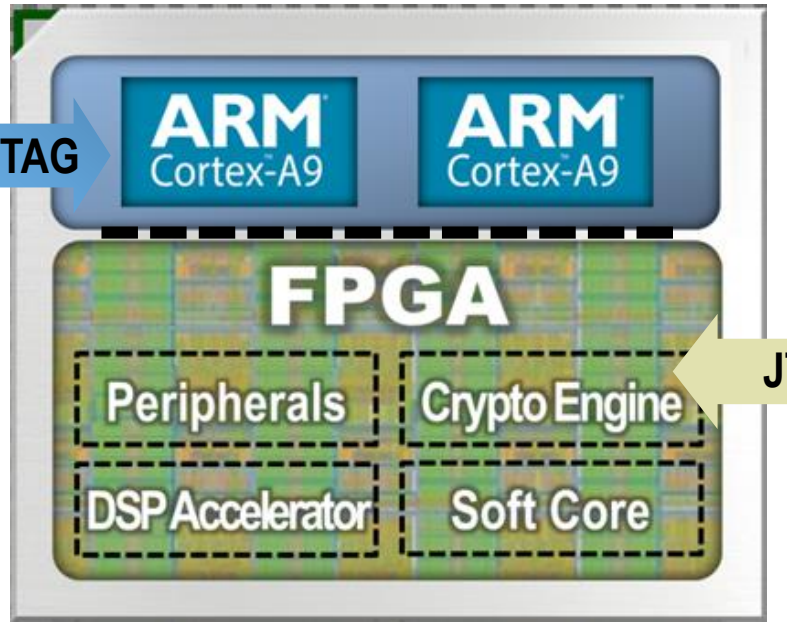


Hardware and software can **co-operate** in debug to visualize where issues cross the SW/HW border

FPGA Logic Analyzer



JTAG



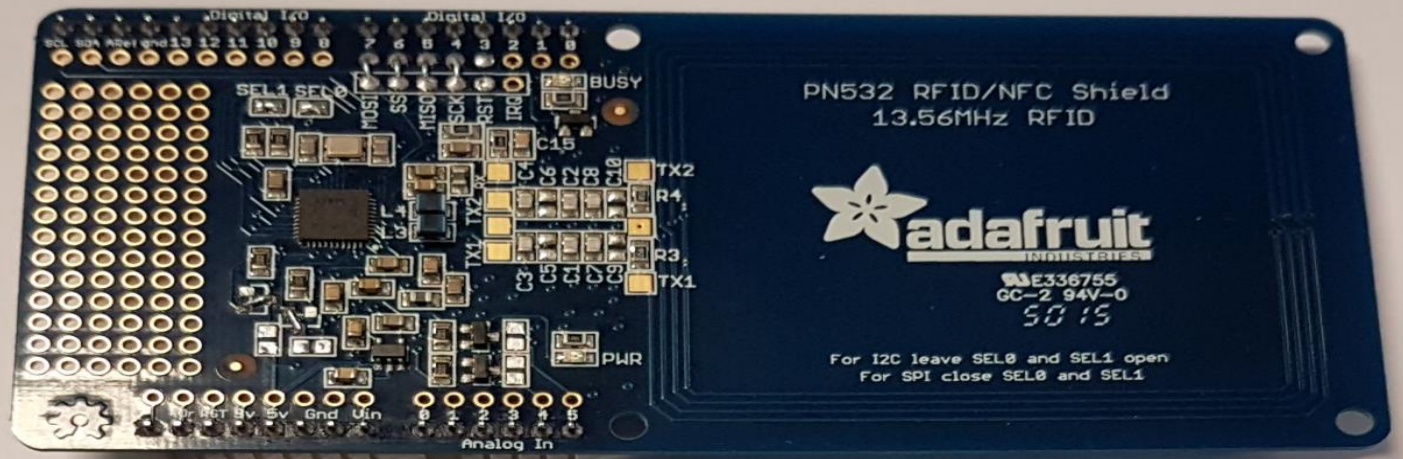
JTAG

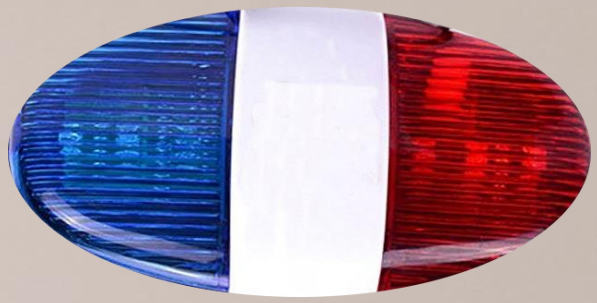
Co-Debugging Demonstration

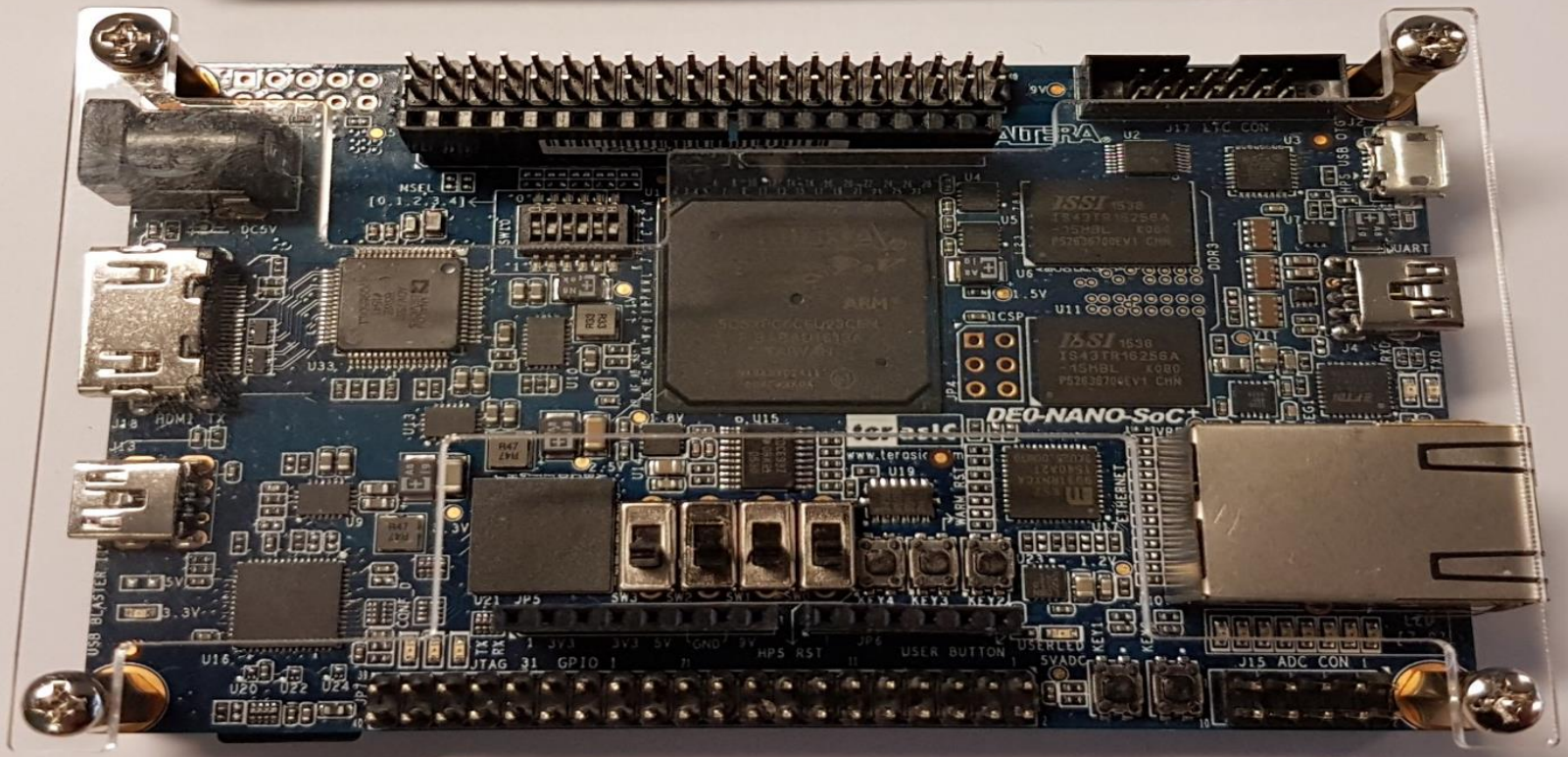
Kris Chaplin

Embedded Technology Specialist
Intel Programmable Solutions Group

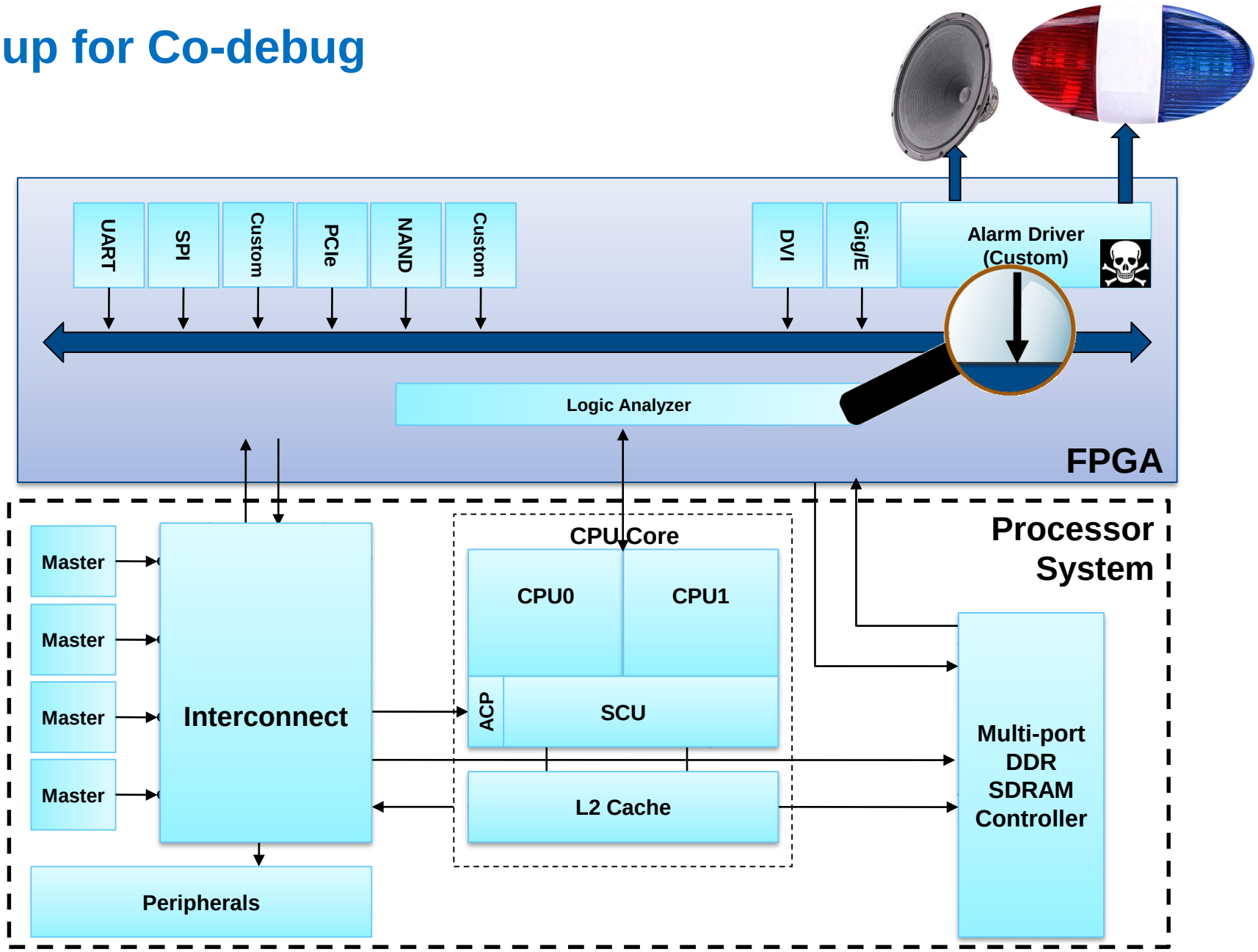
Hardware


PN532 RFID/NFC Shield
13.56MHz RFID
adafruit
INDUSTRIES
E336755
GC-2 94V-0
For I2C leave SEL0 and SEL1 open
For SPI close SEL0 and SEL1
BUSY
PWR
Analog In

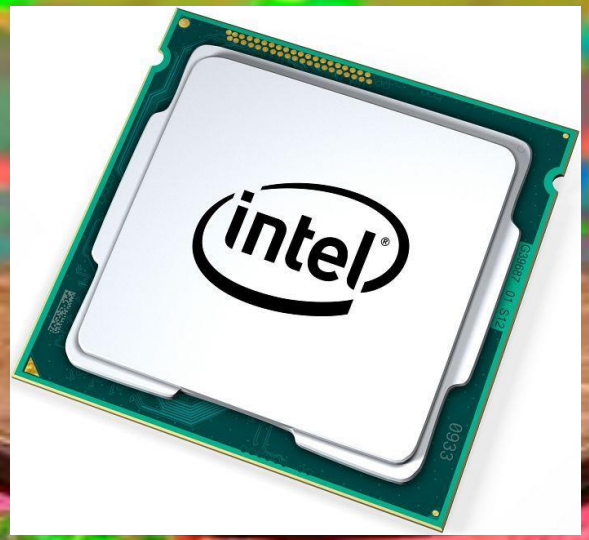


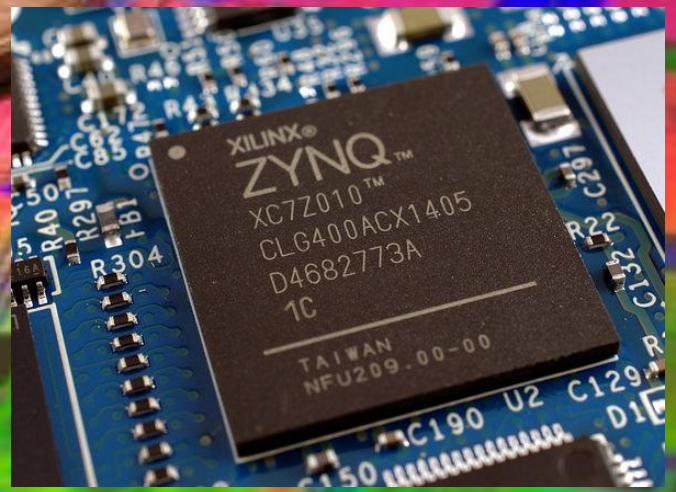

DE0-NANO-SoC
terasIC

Hooking up for Co-debug



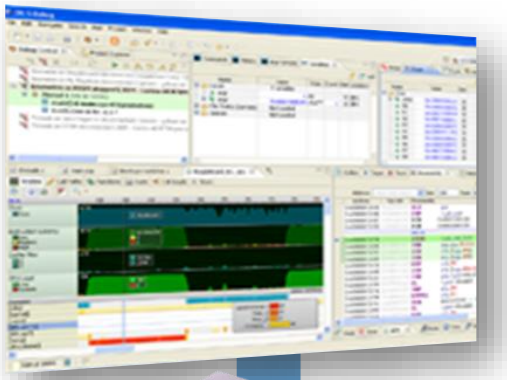
Integration of processors and custom hardware keeps getting tighter, needing tools to integrate too!

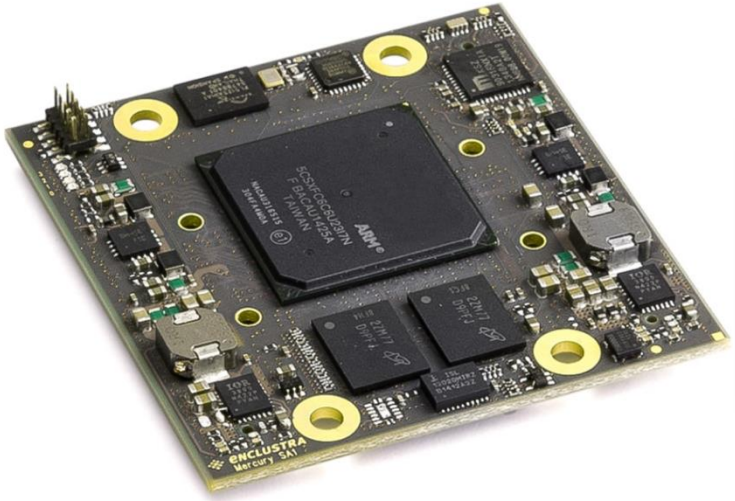




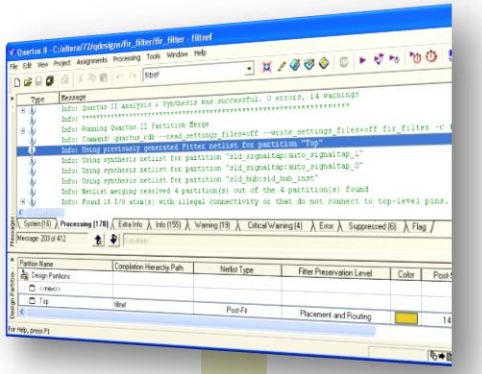
Consider up front how to co-debug hardware and software on your next project - It may save it!

Software JTAG Debugger

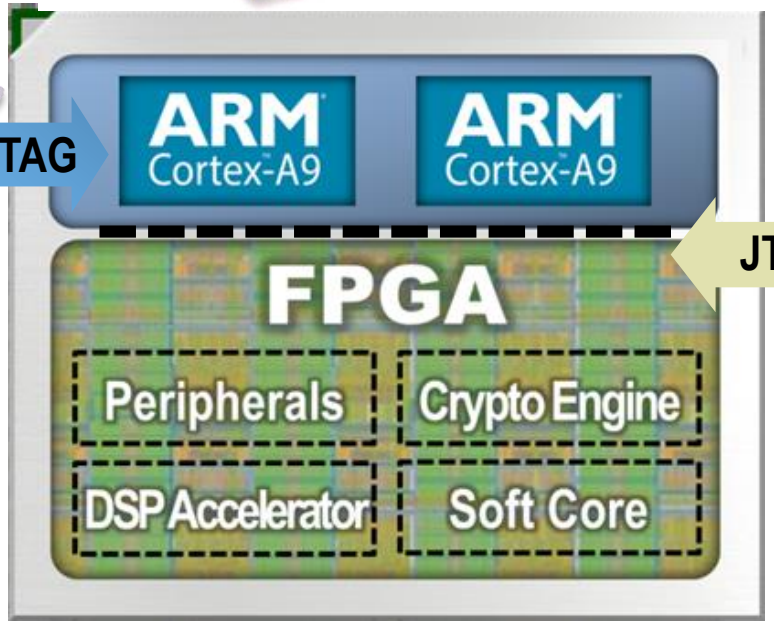




FPGA Logic Analyzer



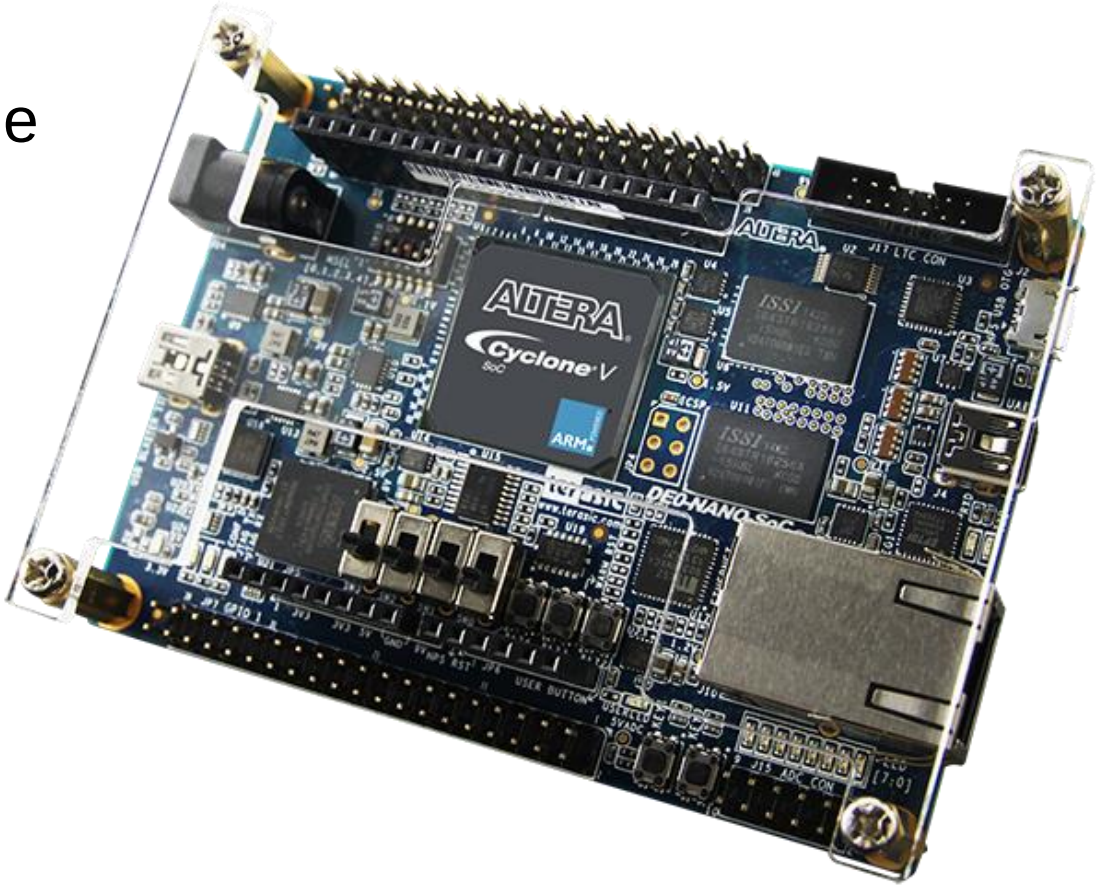
JTAG



JTAG

Altera now part of Intel at ELCE

- Visit the Altera booth at B1 in the technology showcase
- Participate in the Atlas development kit raffle
- Check out Altera's exciting demos!
  - DPD Demonstration
  - Mandelbrot running on Atlas
  - Spider Robot



Thank You