



OpenIoT Summit Europe 2018

Compartmentalization in IoT

Trusted Firmware M
Secure Partitioning

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Arm

Agenda

The right level of security

Hardware support

Compartmentalization scenarios

Interaction between isolated components

Establishing the “right” level of security

Secure domain

Basic isolation – create a Secure Processing Environment

Protected TCB

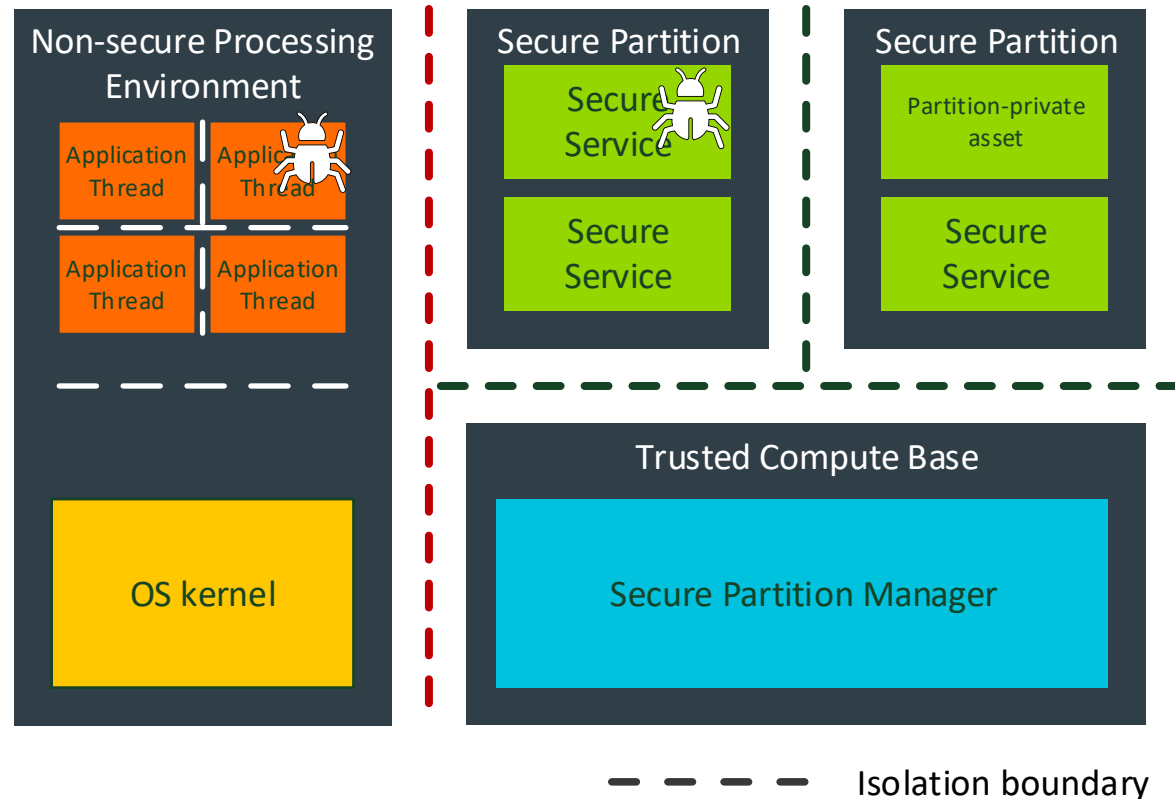
Separate Root of Trust from Secure Partitions within SPE

Multiple tenancy in secure PE

More robustness – isolate all partitions from each other

Non-Secure isolation

Access policies for NS threads



Hardware isolation

... the foundation for software security

Physical isolation (e.g. dual-core system):

Dedicate cores/resources

Shared memory system or Mailbox

Concurrent execution

Temporal isolation (e.g. Arm-v8M):

Privilege control – using MPU

Secure/Non-secure states (Secure Attribution)

Shared Processing Element, resources

Interaction scenarios

Execution flows

Crossing boundaries in single processing element

Crossing from Non-secure to secure state

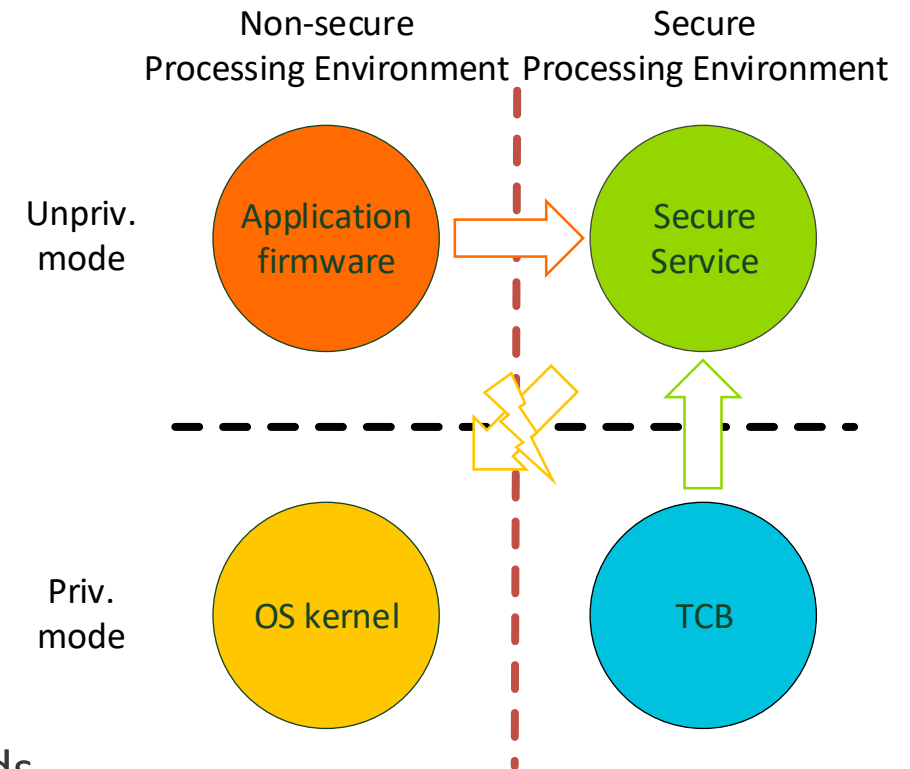
- Non-secure thread requests secure service

Isolated driver code

- ISR execution in unprivileged partition

Asynchronous events in non-secure PE

- Non-secure interrupt pre-empts secure operation
- Non-secure context awareness
- Concurrent secure service requests from non-secure threads



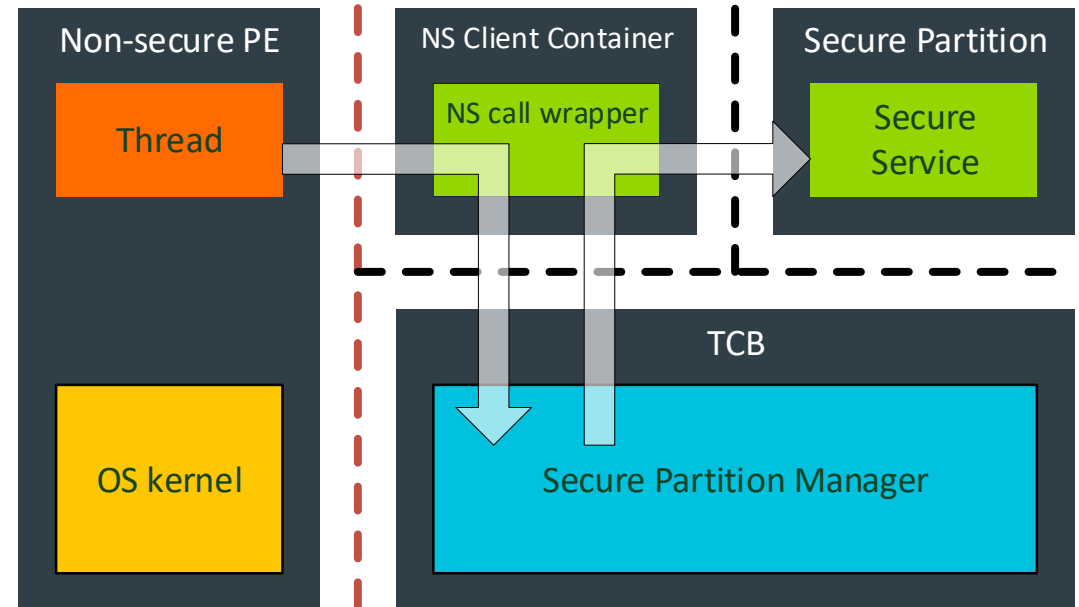
Non-secure call to secure service

Security state change only permitted using dedicated entry points

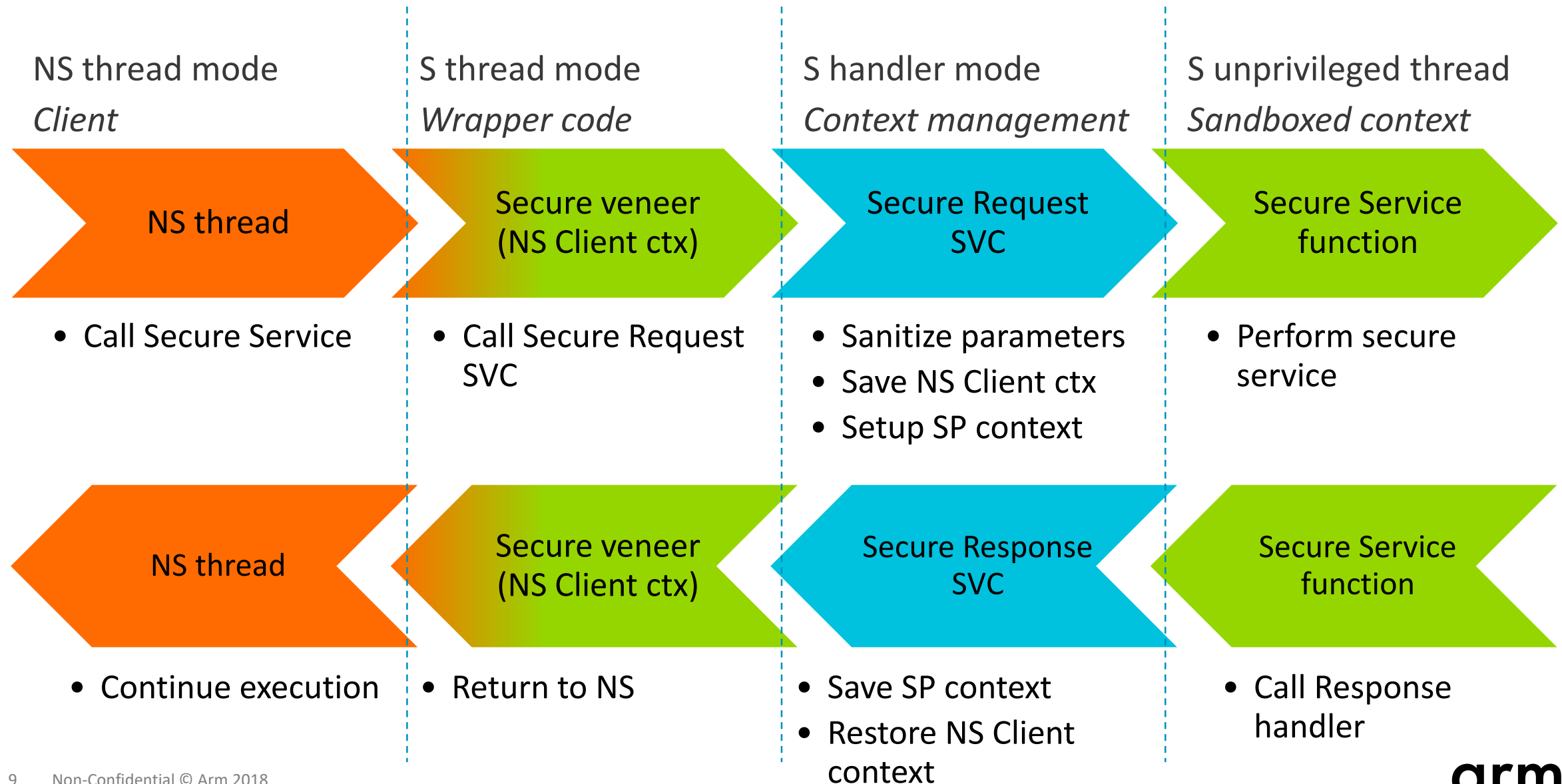
Wrapper function triggers privileged management code

Secure Partition Management code

- Performs parameter sanitization
- Sets up Secure Partition (container)

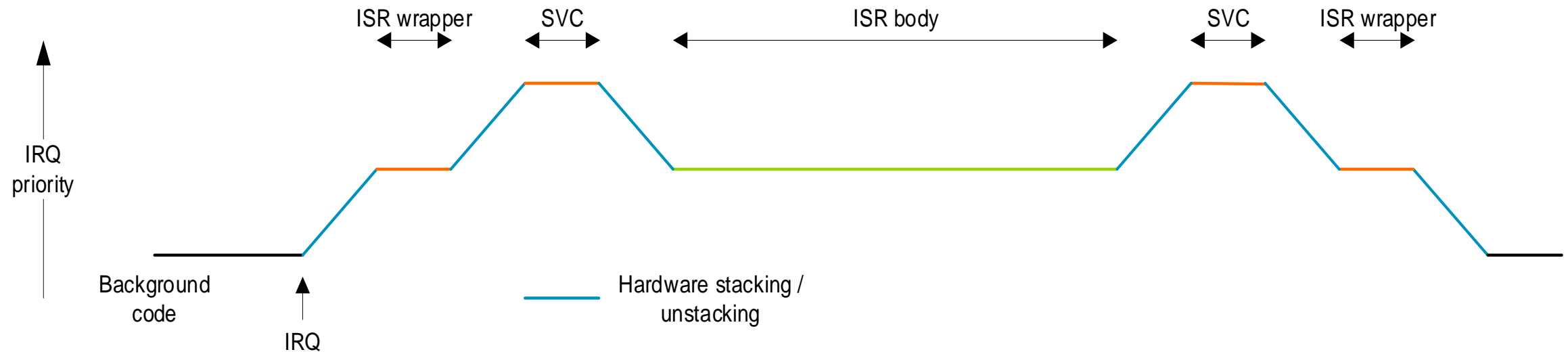


Non-secure call to secure service

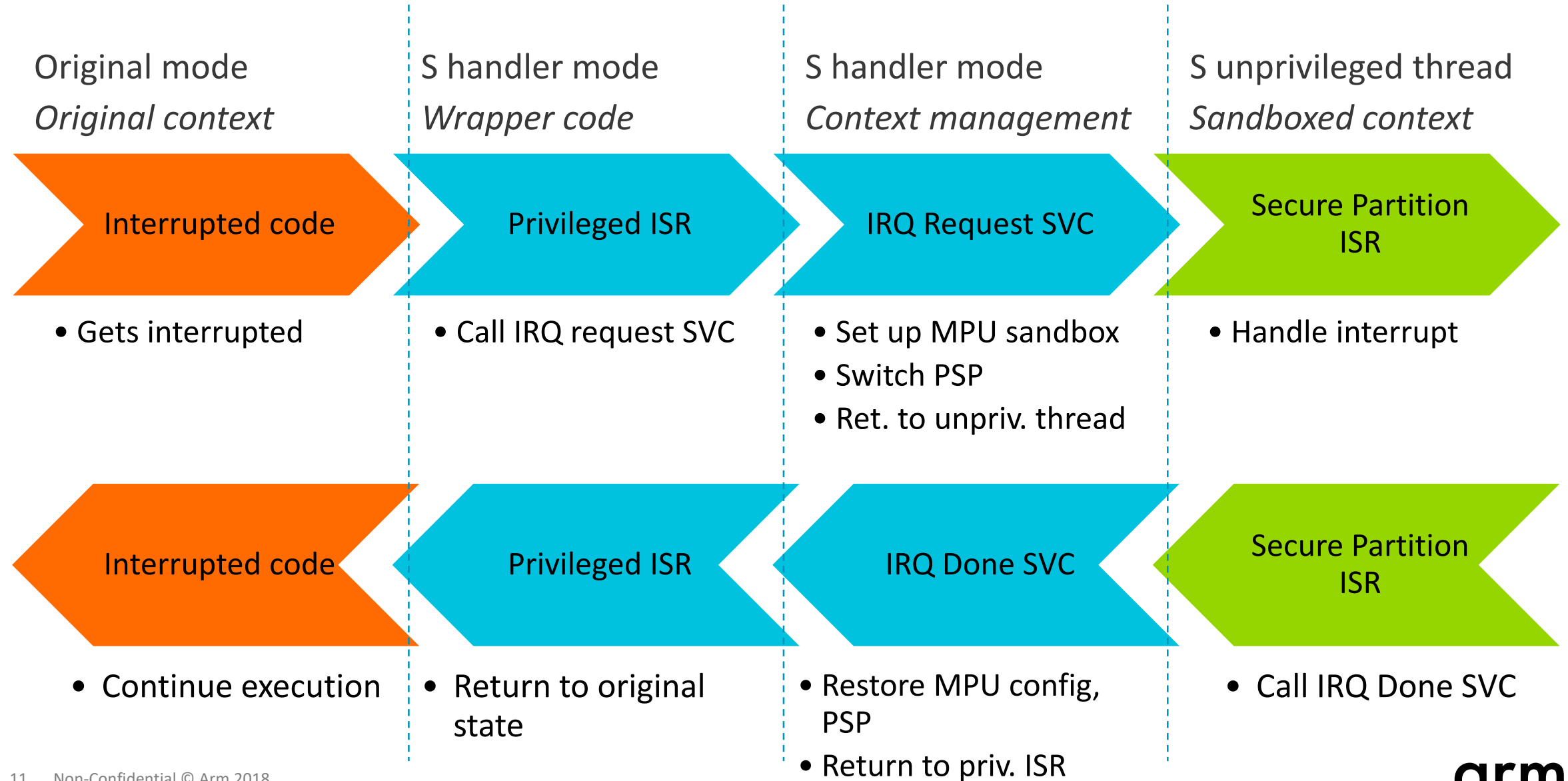


Secure interrupt deprivileging

- Privileged ISR is wrapper
 - Triggers Partition Manager
- Sandbox created
 - Returns to thread mode
- Secure Partition code
 - Executes deprivileged ISR



Secure interrupt deprivileging



Non-Secure interrupts

Pre-emption of secure execution

Non-secure thread is executing

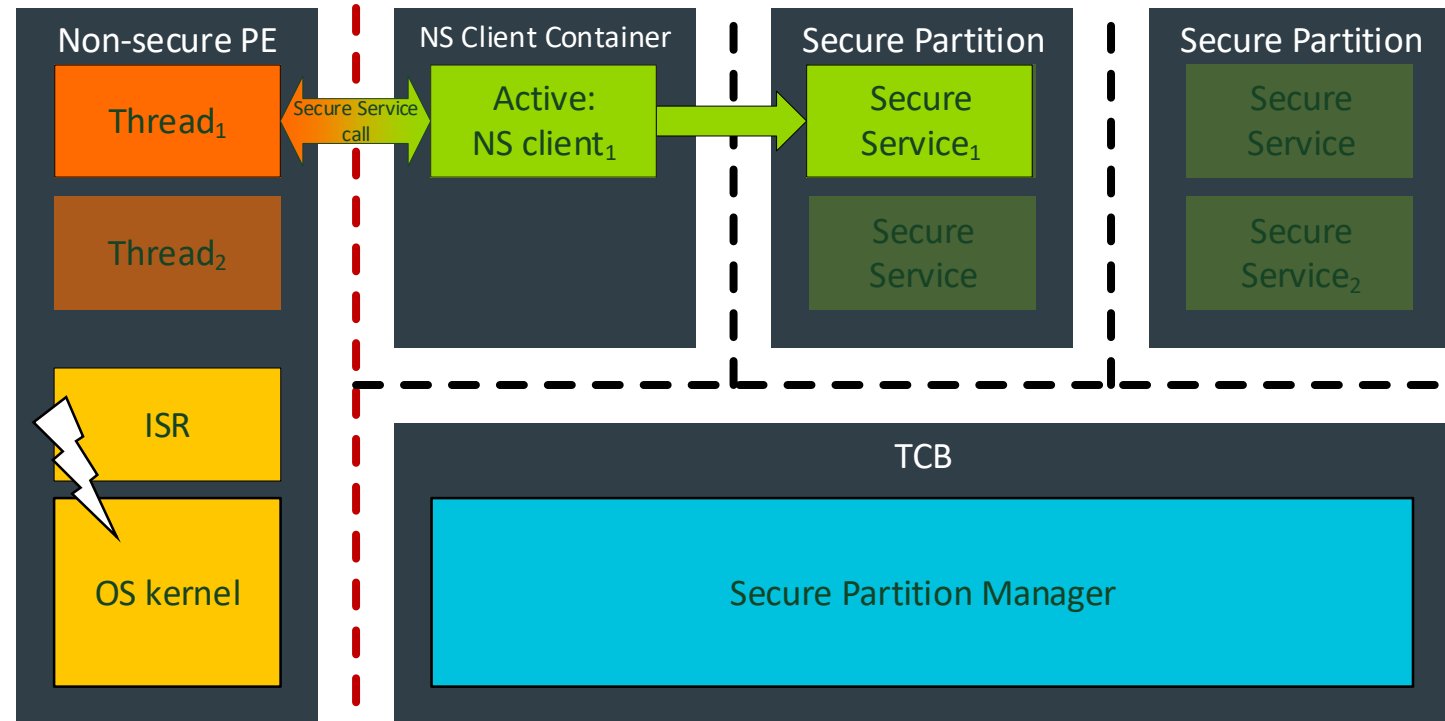
Thread calls Secure Service

Non-secure IRQ pre-empts operation

Secure context is stacked

Non-secure ISR is executed

Return from ISR resumes secure execution

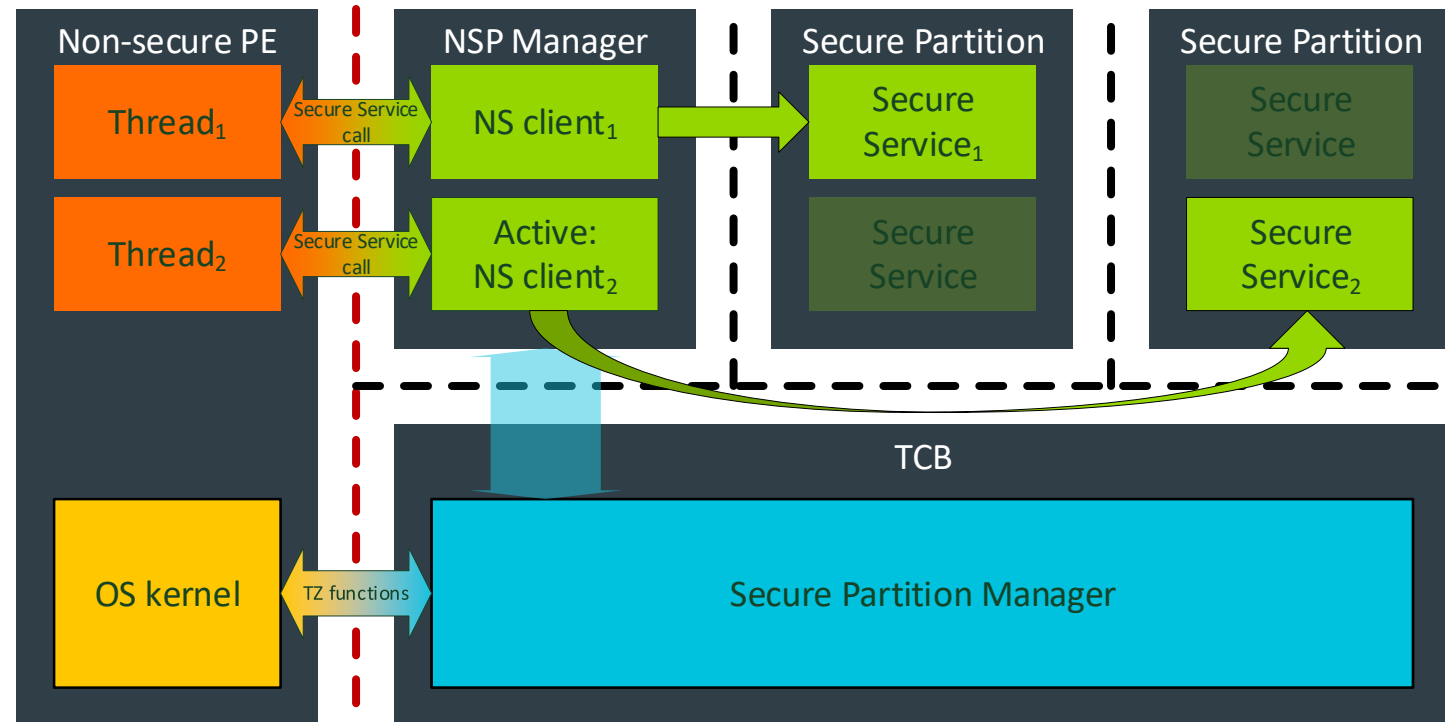


Context Management Functions

Non-secure context awareness in Arm-v8M

1. Non-secure threads created
2. Thread₁ calls Secure Service₁
3. Non-secure IRQ pre-empts operation -> context change
4. Thread₂ calls secure service₂
5. Secure service₂ returns
6. Thread₂ yields
7. Secure Service₁ returns

NS RTOS provides notification to SPM about context creation, deletion, load or store operation, enabling NS context-dependent access to secure assets/services.

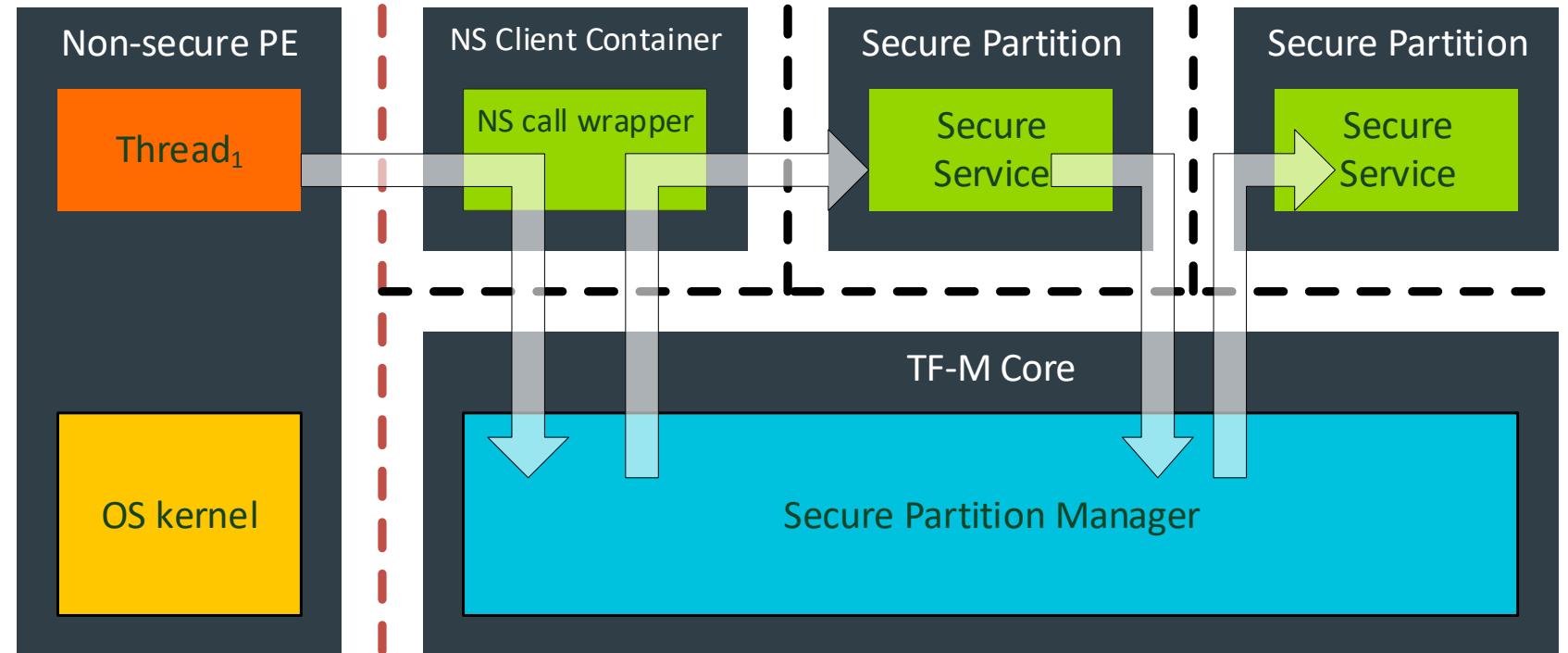


Implementations

Trusted Firmware M library model

Secure Services implemented as functions

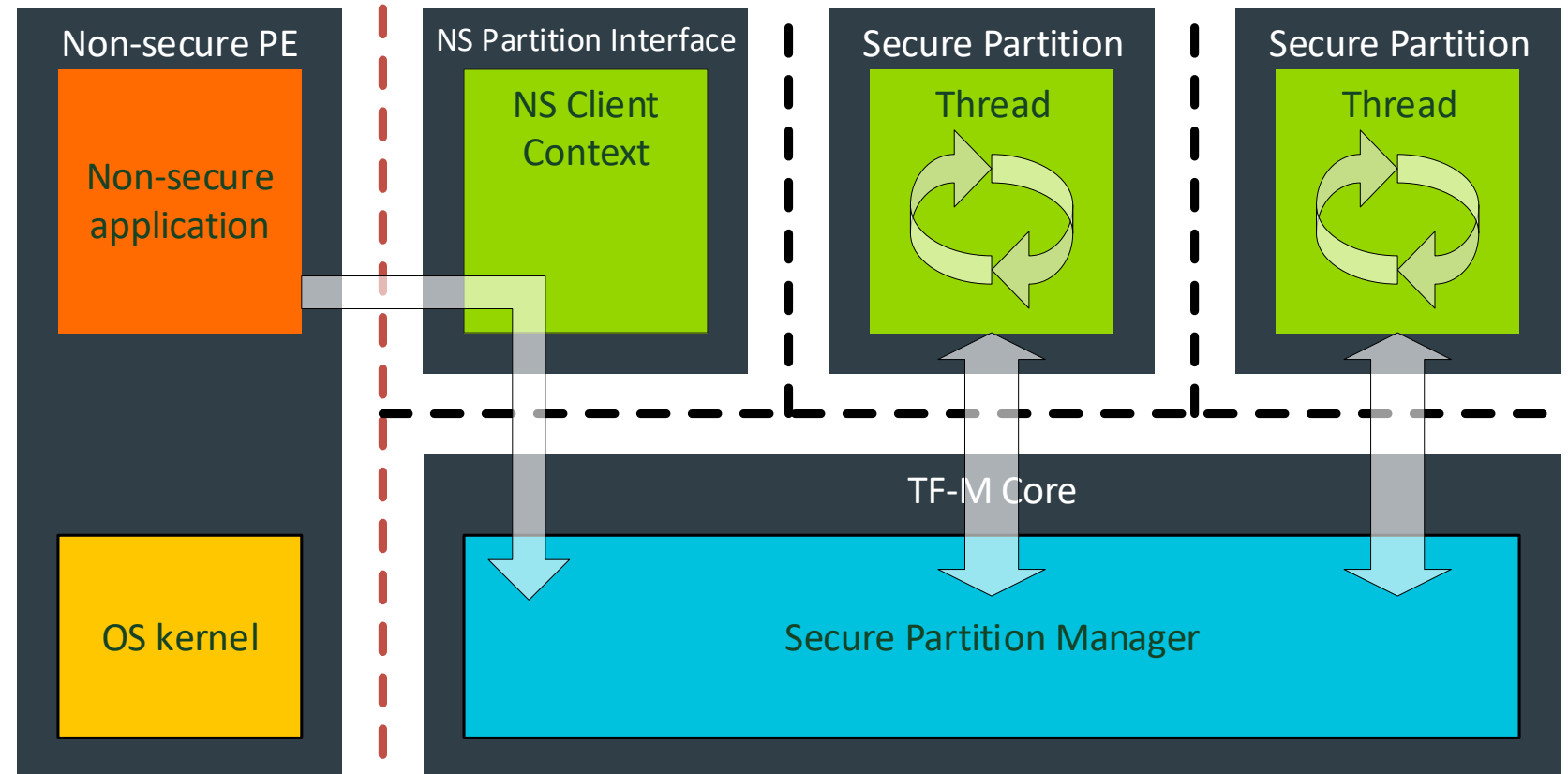
- Arm-v8M architecture support
- Secure Partition is a library of secure services
- Synchronous execution of secure services
- Programming model closely follows embedded/MCU concepts
- Low footprint – on demand allocation of resources



Trusted Firmware M thread model

Secure Partitions implemented as threads

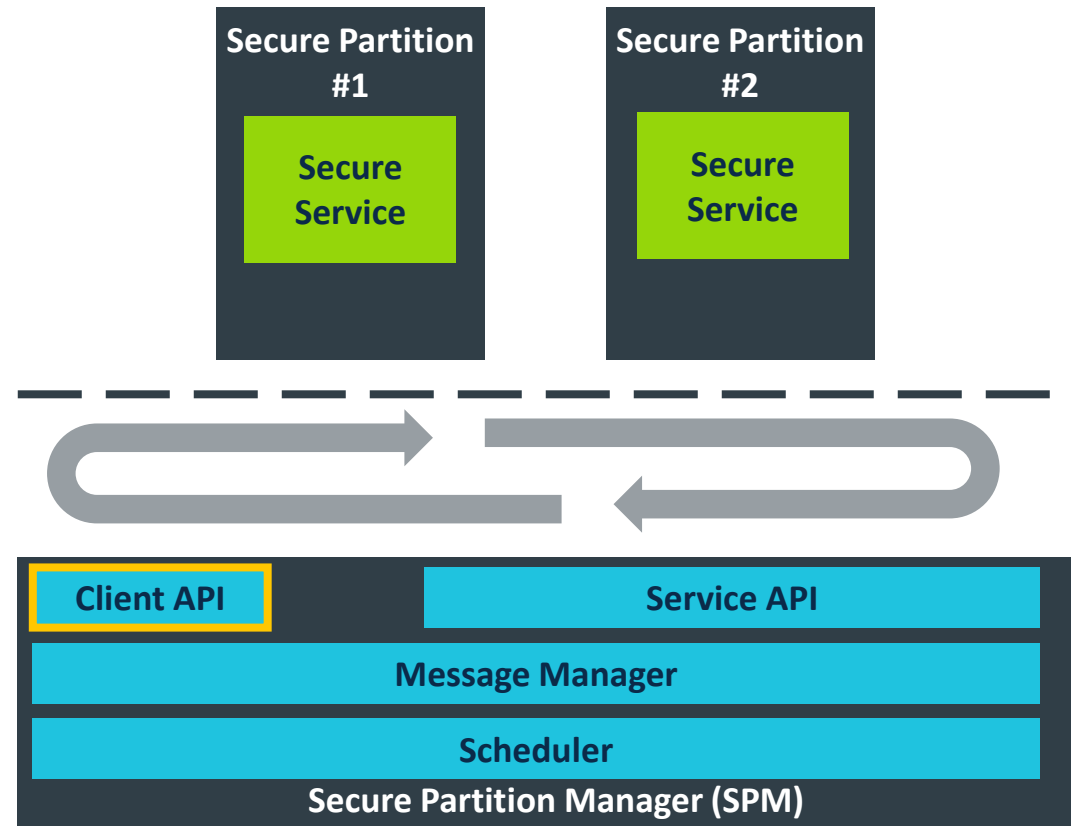
Connection/message based interaction
Robust, more prescriptive framework
Static allocation of secure resources
Asynchronous processing of service requests
Less architecture dependent -> well suited for physical separation



Interaction with secure threads

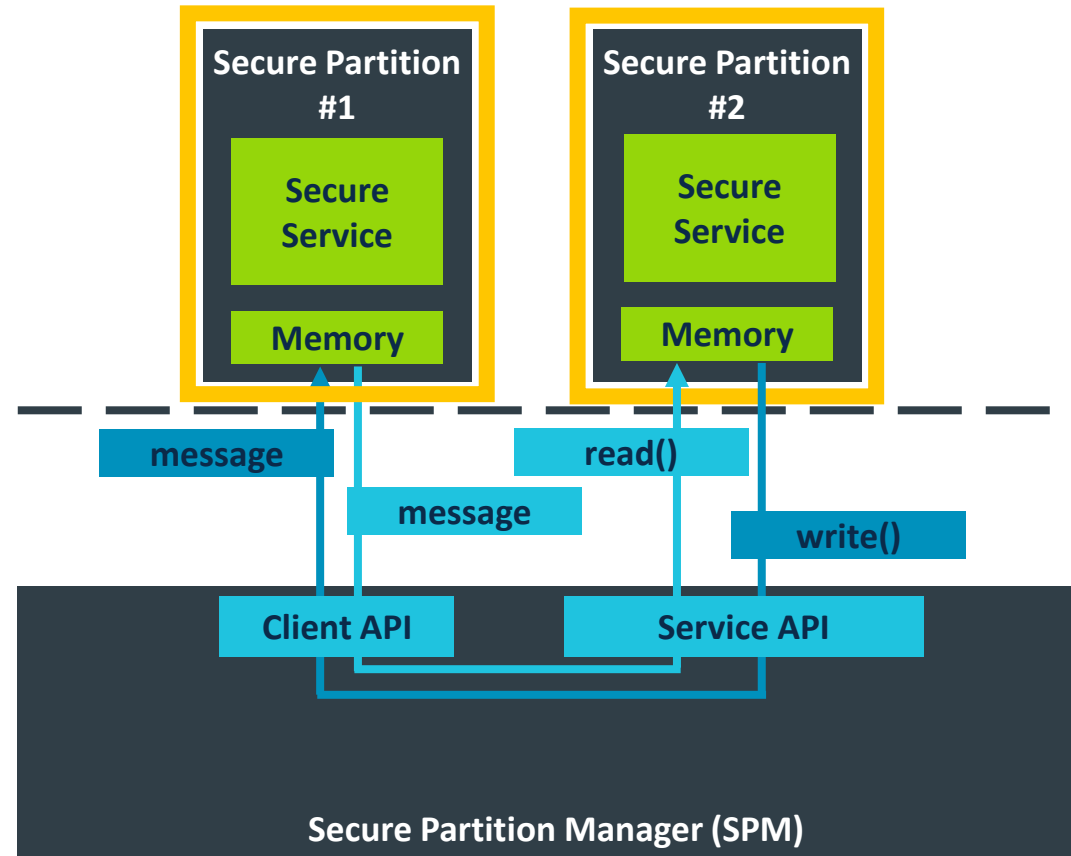
TF-M Inter-Process Communication (IPC)

- For TF-M Thread model
- Secure Partitions provide secure services
 - NSPE is reflected as one Non-Secure Partition
- One thread in one Secure Partition
- While loop in thread waiting for messages
- Client call sent as messages
 - Non-Secure Partition is a client
 - Secure Partition could be a client
- Service Interrupt is handled asynchronously

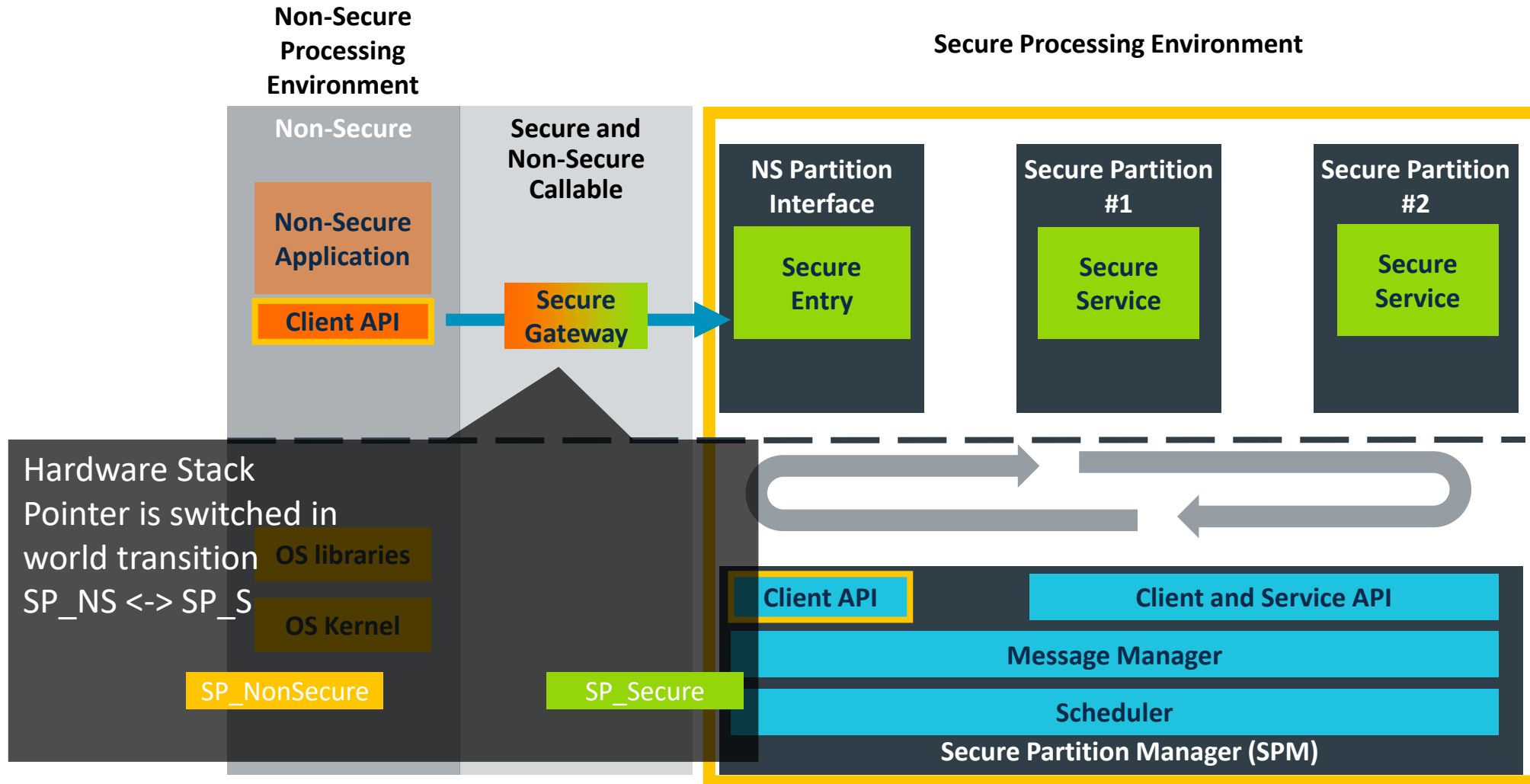


Security Consideration on Compartmentalization

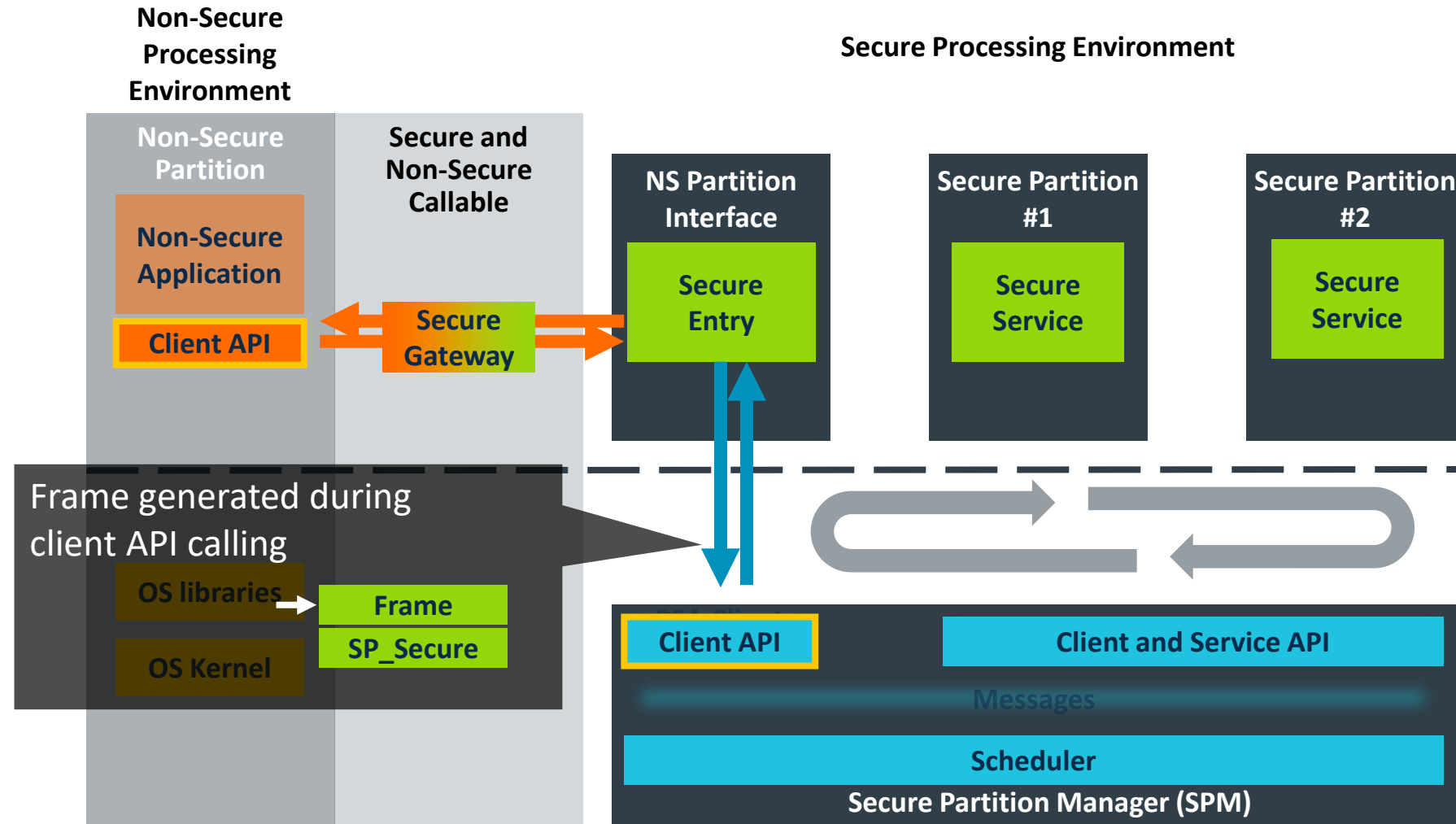
- No shared memory
- Streamed read/write APIs for copying memory
- Memory integrity checking based on isolation level
- Peripheral usage is also isolated
- Runtime protection rule change to isolate



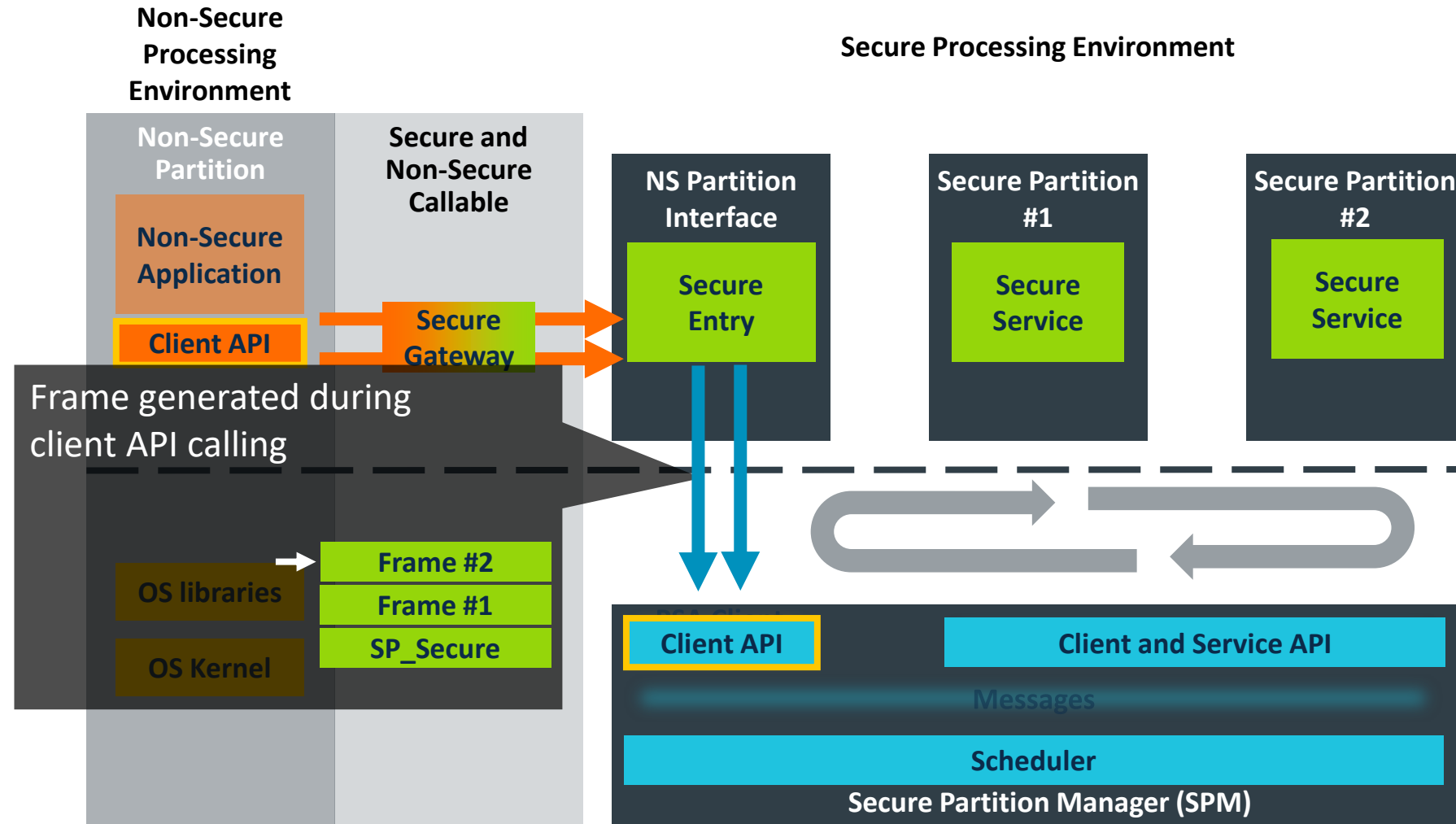
Expand NSP with Arm-v8M TrustZone



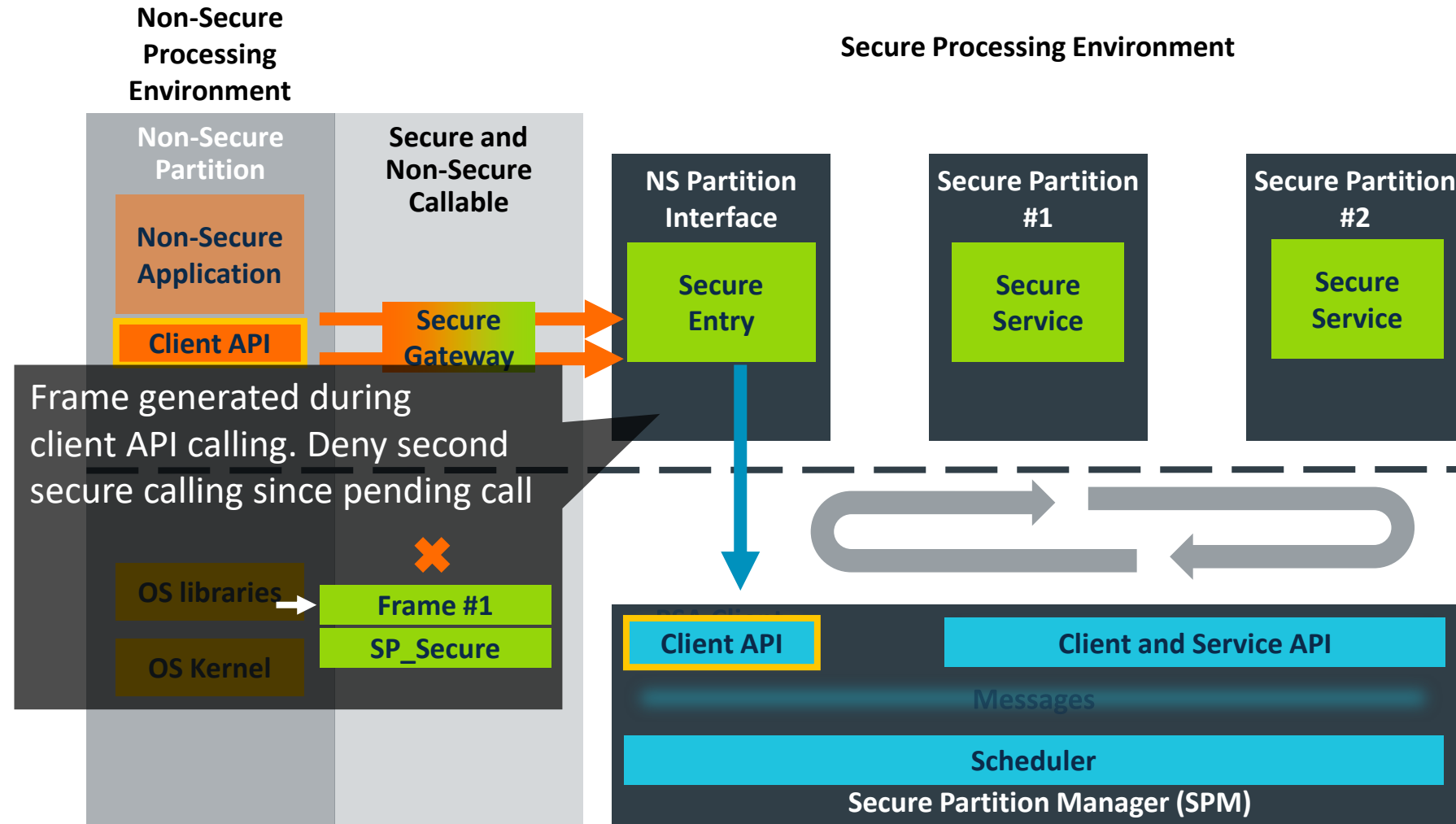
Single NS Thread requests Secure Service



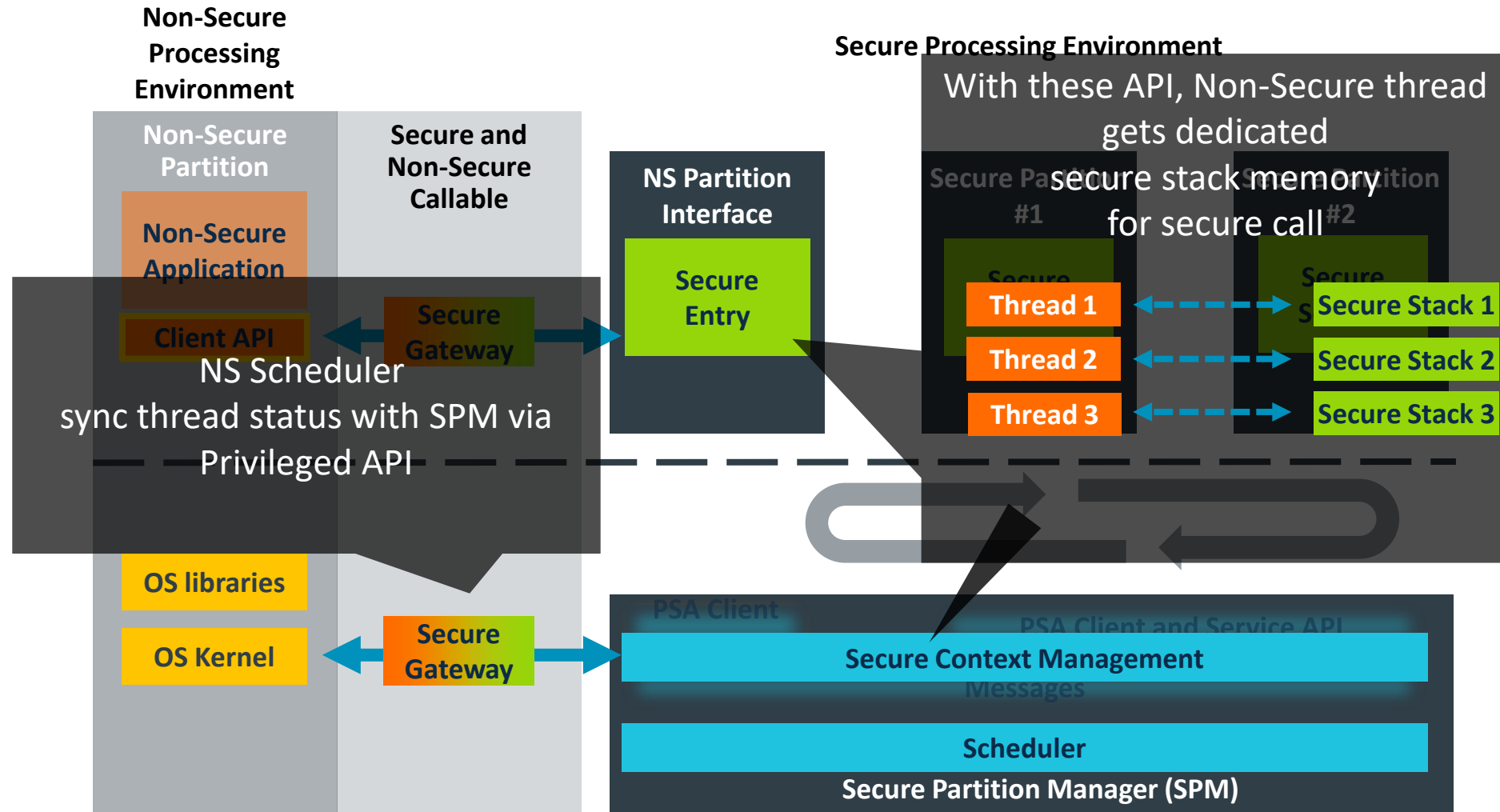
Multiple NS Thread request Secure Service



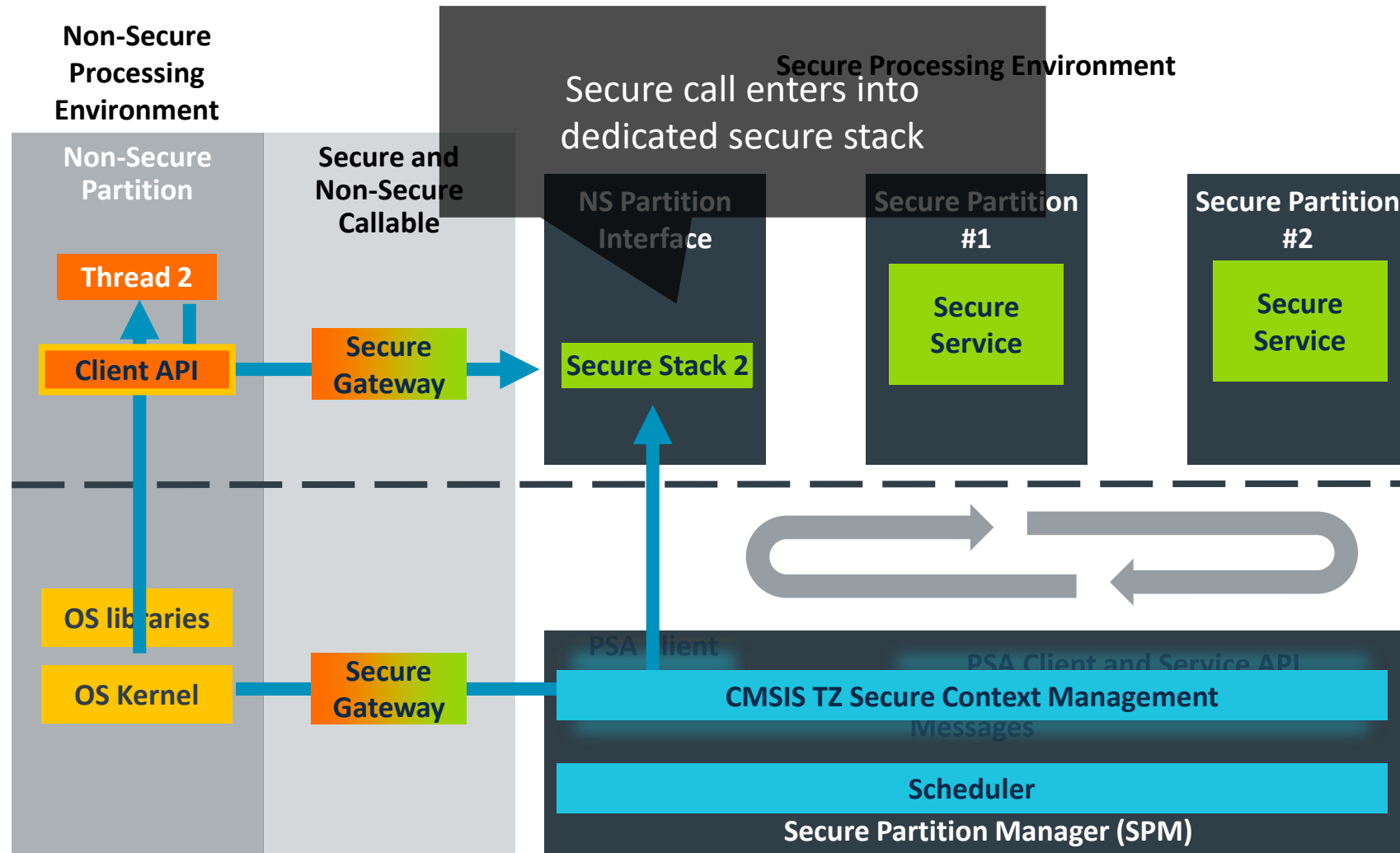
Multi-Thread NSPE Secure Call Solution 1



Multi-Thread NSPE Secure Call Solution 2

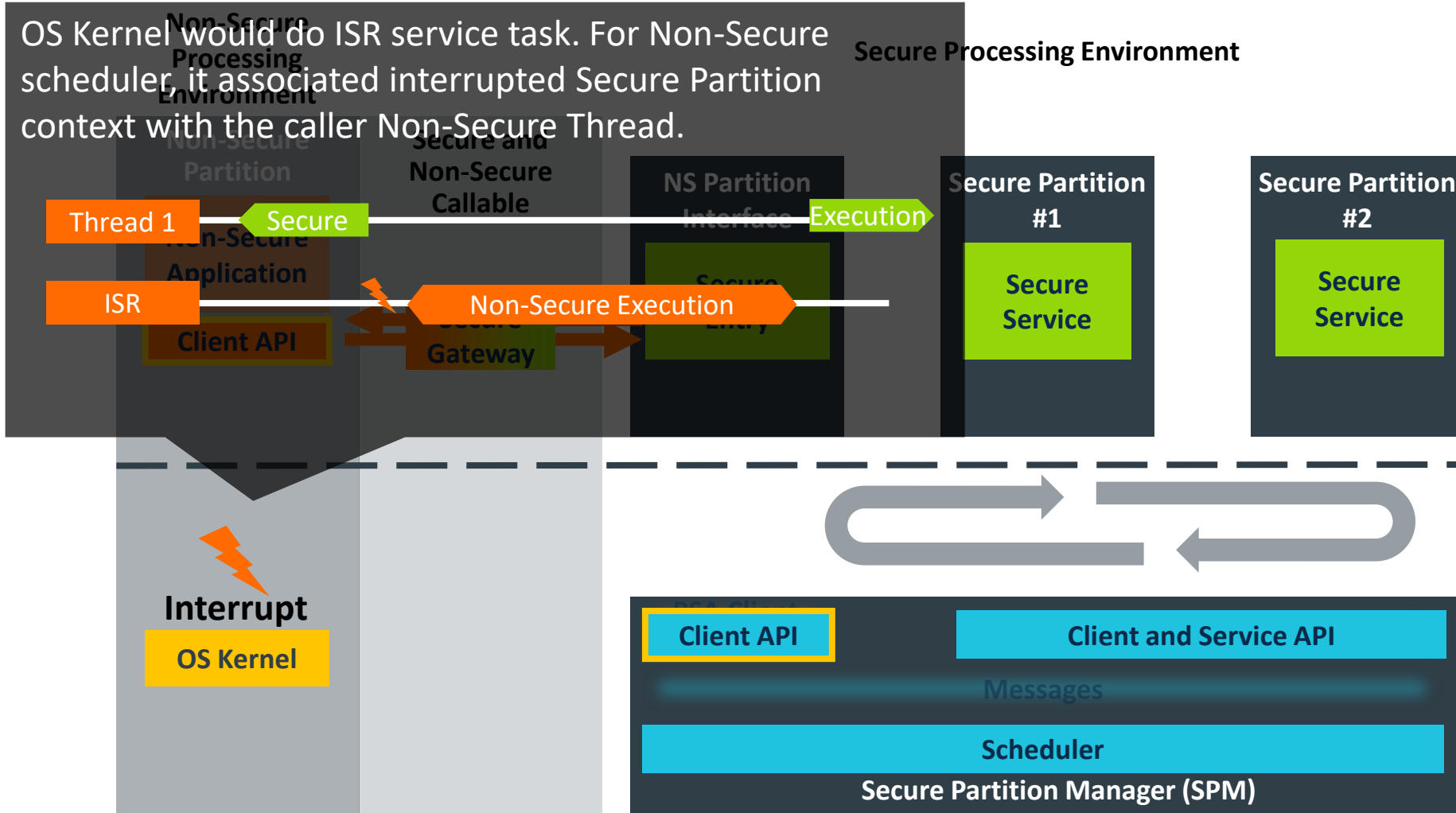


Solution 2 Calling Process

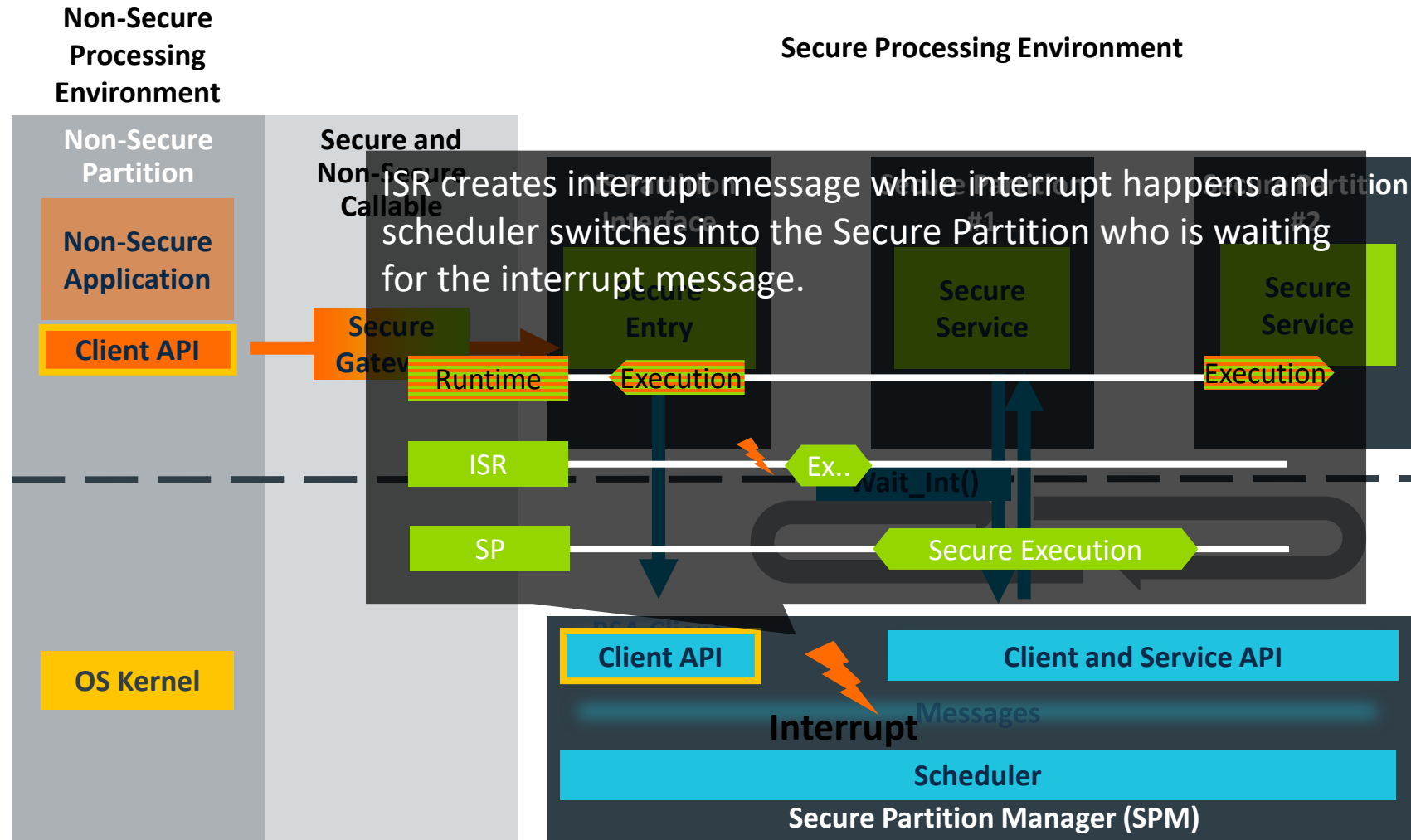


Non-Secure Interrupt Preempts Secure Service

OS Kernel would do ISR service task. For Non-Secure scheduler, it associated interrupted Secure Partition context with the caller Non-Secure Thread.



Secure Interrupt Preempts Execution



Summary

How to get involved

TF-M is part of the Open Source/Open Governance trustedfirmware.org project

- Code base: <https://git.trustedfirmware.org/>

TF-M Team @ OpenIoT Summit Europe 2018

- Shebu Kuriakose
- Ashutosh Singh
- Ken Liu
- Miklos Balint

Get in touch

- Come round to the Arm booth during the summit
- Contact TF-M team at support-trustedfirmware@arm.com

More info on developer.arm.com and trustedfirmware.org

Thank You!

Danke!

Merci!

谢谢!

ありがとう!

Gracias!

Kiitos!

감사합니다

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