Slides: tinyurl.com/elc2023-bof

EMBEDDED LINUX CONFERENCE

ELC Prague 2023

RISC-V and Open Hardware BoF

Drew Fustini <dfustini@baylibre.com>

$ whoami

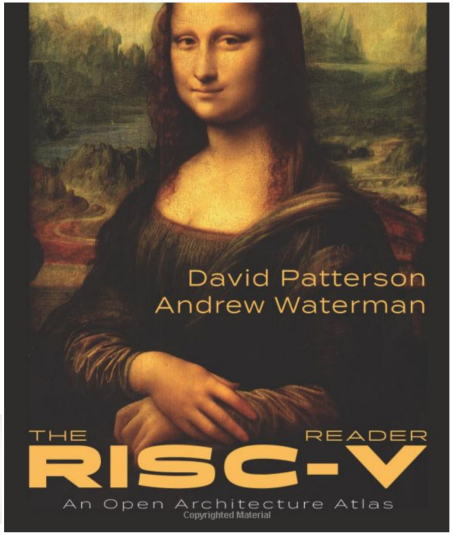
- Linux kernel developer, BayLibre
  - embedded software consultancy based in Nice, France, with ~50 engineers around the world contributing to open source projects like Linux, U-Boot, Android and Zephyr
- Board of Directors, BeagleBoard.org Foundation
- Ambassador, RISC-V International
- Member, FOSSi Foundation and Open Source Hardware Association

RISC-V: a Free and Open ISA

- Started by a computer architecture research group at University of California Berkeley in 2010 led by Krste Asanovic
- **V** as in the roman numeral five, because it is the 5th **RISC** instruction set to come out of UC Berkeley
- **Free and Open** because the specifications are published under an open source license: Creative Commons Attribution 4.0 International
  - Volume 1, Unprivileged Spec v. 20191213 [PDF]
  - Volume 2, Privileged Spec v. 20211203 [PDF]

Learn more about RISC-V

- Get up-to-speed quick with the RISC-V Reader



RISC-V International

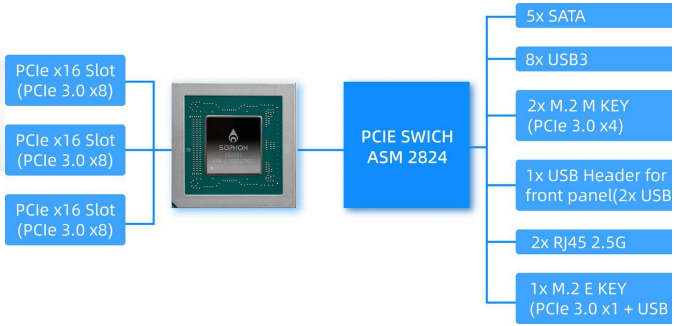
- The organization that develops the RISC-V specifications: **riscv.org**
- Non-profit with 2,700+ members including companies and universities
- Become a member - *free of cost to individuals and non-profits*
- RISC-V wiki has many helpful resources
- RISC-V mailing lists for many topics *(public archives)*
- Technical Meetings Calendar

RISC-V Developer Boards

- Initiative from RISC-V International to get Linux-capable boards into the hands of open source developers
  - Need to be RISC-V International member (or part of a member organization), but remember that individuals can join RISC-V International free of cost
- Currently accepting applications for:
  - Milk-V Pioneer Box featuring 64 core Sophgo SoC and 128 GB memory (!!!)
  - StarFive VisionFive V2 board

MilkV Pioneer with 64 cores!

- Sophgo SOPHON SG2042 has 64-core T-Head C920 @ 2 GHz
- CrowdSupply campaign just launched, ships December 2023
  - $1,199 for Milk-V Pioneer motherboard
  - $1, 999 for Milk-V Pioneer Box 128 GB ram, 1 TB SSD, 2x 10Gb Ethernet, AMD R5 230 GPU



Sipeed Lichee Pi 4A

- Alibaba T-Head TH1520 SoC with 4x C910 cores (12-stage, out-of-order)
- $119 on AliExpress

Recent RISC-V presentations

- Linux on RISC-V *(ELC-E 2022 Dublin)*
- RISC-V YouTube channel
  - State of the Union & the Road Ahead
  - Maturing the RISC-V Ecosystem
  - Evolving the Role of Software in the RISC-V Ecosystem
  - **RISC-V Summit Europe (May 2023) videos coming soon…**

“Is RISC-V an Open Source processor?”

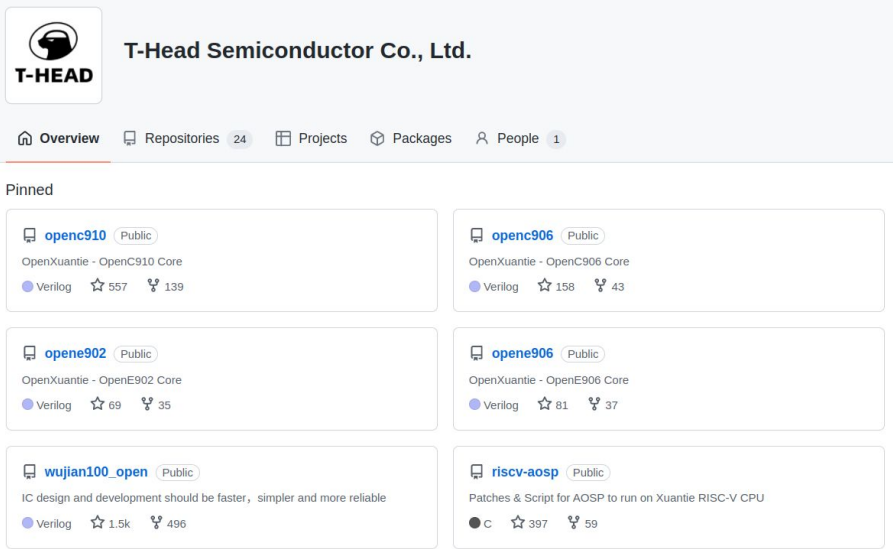
- RISC-V is a set of specifications under an open source license
- RISC-V implementations can be open source or proprietary
- Open specifications make open source implementations possible
- **An open ISA makes it possible to design an open source processor**

RISC-V open source cores

- Academia
  - Rocket and BOOM from Berkeley, PULP family of cores from ETH Zurich
- Industry
  - OpenHW Group creating proven verified IP like their Core-V designs
  - OpenTitan silicon root of trust project uses LowRISC Ibex core
  - SweRV created by Western Digital and now developed by CHIPS Alliance
- FPGA friendly
  - PicoRV32, RVfpga, SERV, VexRiscV, NaxRiscv

Alibaba T-Head open source RISC-V cores

- OpenE902, OpenE906, OpenC906 (used in Allwinner D1 SoC), and OpenC910 cores on GitHub under permissive Apache 2.0 licence




```
|--C910_RTL_FACTORY/
  |--gen_rtl/     ## Verilog source code of C910
  |--setup/       ## Script to set the environment variables
|--smart_run/     ## RTL simulation environment
  |--impl/        ## SDC file, scripts and file lists for implementation
  |--logical/     ## SoC demo and test bench to run the simulation
  |--setup/       ## GNU tool chain setting
  |--tests/       ## Test driver and test cases
  |--work/        ## Working directory for builds
  |--Makefile     ## Makefile for building and running sim targets
|--doc/           ## The user and integration manual of C910
```

XiangShan (香山)

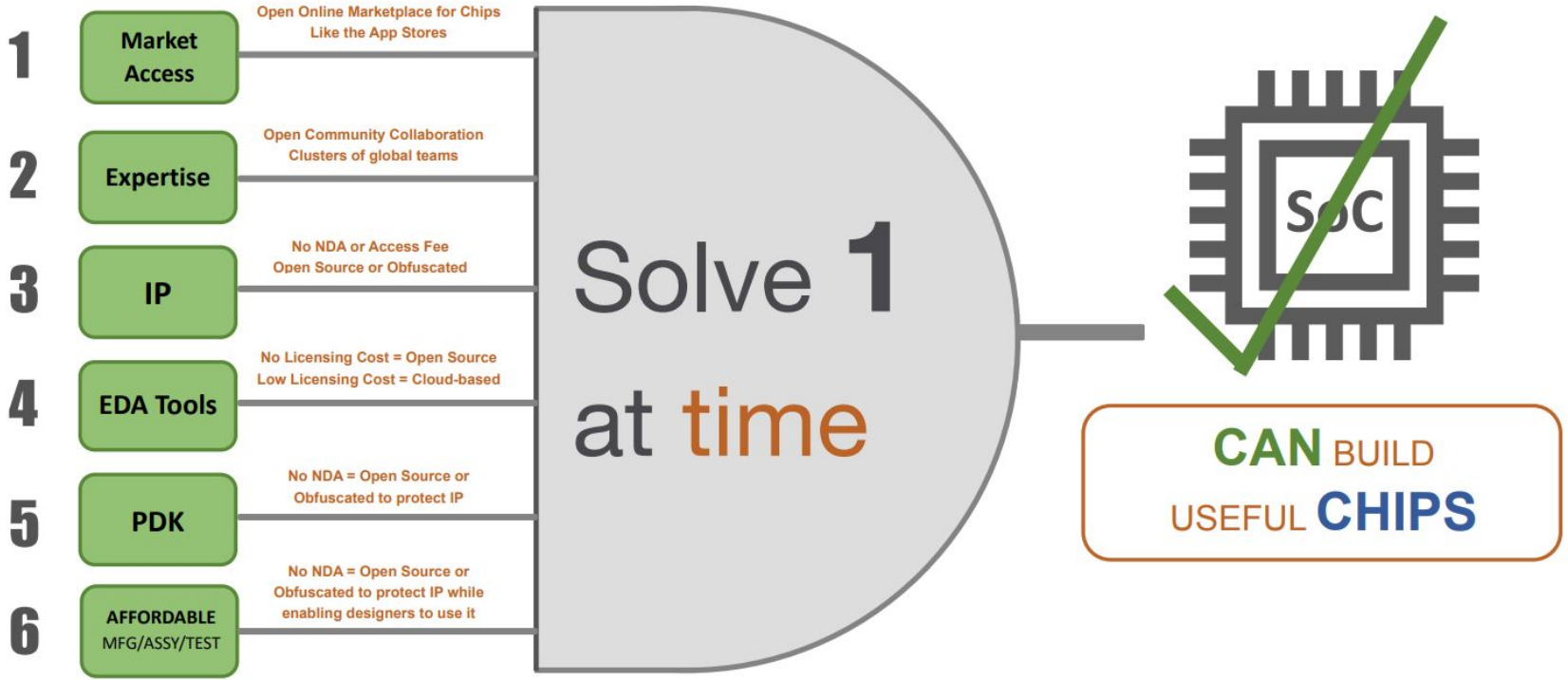
- open source high-performance RISC-V processor project from the Chinese Academy of Science
- RISC-V Summit 2021 talk by Professor Yungang Bao (slides)
  - "Contribute to XiangShan and realize your ideas on real chips! The open-source XiangShan will be taped-out every ~6 months"
  - *RISC-V Summit Europe (May 2023) should be posted soon…*
- Nanhu is the 2nd generation microarchitecture
  - Target: 2GHz@14nm, SPEC CPU2006 20 marks; 7.81 CoreMark/MHz

Open source silicon

- FOSSi Foundation (Free and Open Source Silicon)
  - El Correo Libre monthly newsletter for the latest on open source cores
- Build your own open source SoC with an open source silicon toolchain
  - Google and eFabless worked with Skywater to open source their 130 nm PDK (process design kit) and more recently 90 nm process; also GlobalFoundries180nm PDK too
  - Google sponsored free-of-cost MPW (multi-project wafer) for open source projects
  - Zero to ASIC course: learn to design your own chip using open source design tools
  - Tiny Tapeout: design your own simple chip in web browser and get it made for $100

"Design and Funding Your Custom ASIC in Three Months", **Mohamed Kassem** of eFabless, at Teardown 2023 (video)

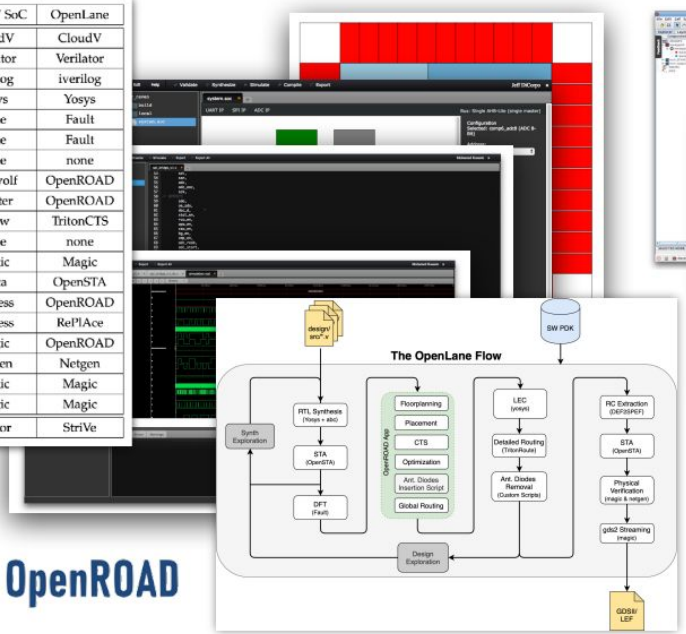
….. what we need …



"Design and Fund Your Custom ASIC in Three Months", **Mohamed Kassem** of eFabless, at Teardown 2023 (video)

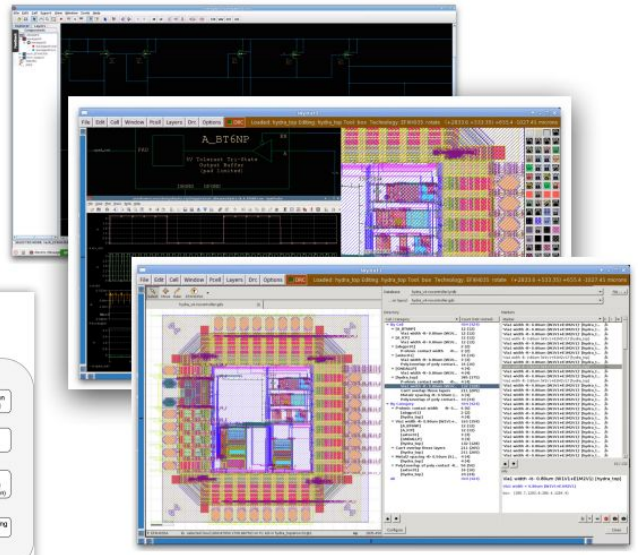
OPEN SOURCE DESIGN FLOWS & TOOLS

DESIGN STEP	Qflow	CloudV SoC	OpenLane
System Design	N/A	CloudV	CloudV
RTL Lint	Verilator	Verilator	Verilator
RTL Simulation	iverilog	iverilog	iverilog
Logic Synthesis	Yosys	Yosys	Yosys
DFT Scan Insertion	none	none	Fault
DFT ATPG	none	none	Fault
Formal Verification	none	none	none
Placement	graywolf	graywolf	OpenROAD
Routing	qrouter	qrouter	OpenROAD
CTS	Qflow	Qflow	TritonCTS
Dynamic EMIR	none	none	none
Extraction	Magic	Magic	Magic
Timing Analysis	Vesta	Vesta	OpenSTA
Floorplanning	Magic	efabless	OpenROAD
Top-Level Placement	Magic	efabless	RePlAce
Top-Level Routing	Magic	Magic	OpenROAD
LVS	Netgen	Netgen	Netgen
DRC	Magic	Magic	Magic
GDS	Magic	Magic	Magic
SoC	Raven	Raptor	StriVe



- SoC Editor
- RTL Simulation
- Synthesis
- GL Simulation

OpenROAD



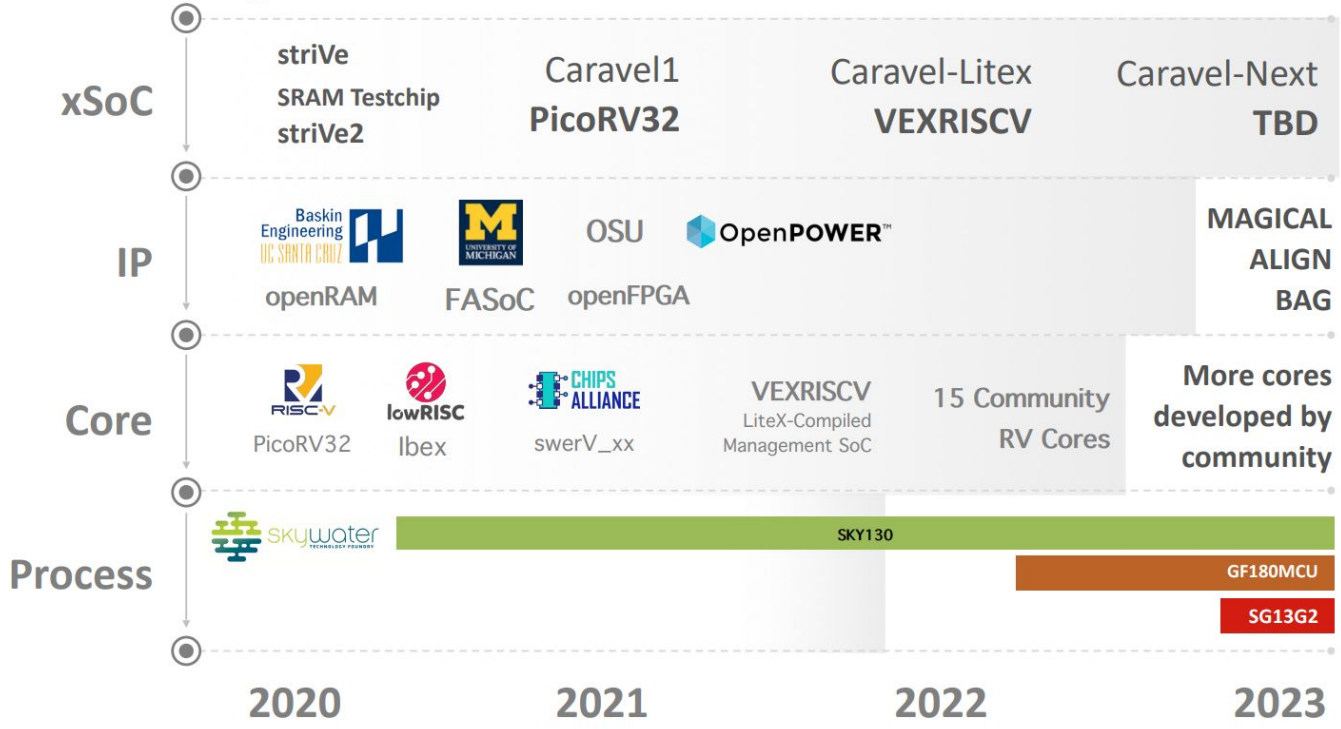
- Schematic Capture
- SPICE Simulation
- Mixed-Mode Simulation
- Parasitic Extraction
- Physical Verification

Silicon Compiler Coriolis OpenLane

efabless.com

"Design and Fund Your Custom ASIC in Three Months", **Mohamed Kassem** of eFabless, at Teardown 2023 (video)

A library of IP blocks - Go Build It



efabless.com

"Design and Fund Your Custom ASIC in Three Months", **Mohamed Kassem** of eFabless, at Teardown 2023 (video)

Open Source technology PDKs

No NDA, nothing to sign - it's Open Source

2020 skywater TECHNOLOGY

FOSS 130nm Production PDK
github.com/google/skywater-pdk

2022 GLOBAL FOUNDRIES

FOSS 180nm Production PDK
github.com/google/gf180mcu-pdk

2023 ihp

SG13G2 BiCMOS 0.13µm PDK
github.com/IHP-GmbH/IHP-Open-PDK

Technology PDK availability is virtually limitless

*Leading to **massive open collaboration***

GOOGLE's OPEN MPW PROGRAM

efabless.com
Sponsored by Google

- **Google** is funded **8** manufacturing runs in **2021/22**
- Participants use an Harness SoC (Caravel) with ***10mm2 open area***
- SKY130 Open Source Digital & Analog Design Tools are available
- Participants get ***5 dev boards + 300 WCSP-packaged parts***
- All designs must be public and under an ***open source license***
- All designs must contain information & files to ***reproduce the work***
- Participants are strongly encouraged to try new ideas, ***take risks and iterate***
- All skill and experience levels are welcome to participate

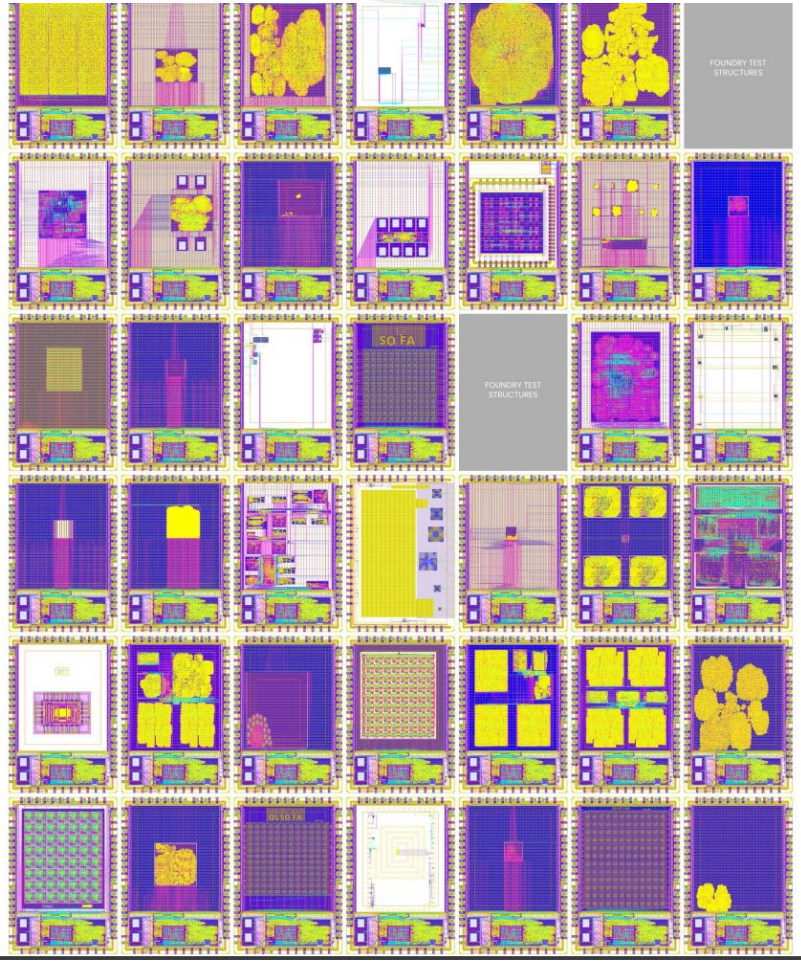
Start here https://ef.link/gmpw

"Design and Fund Your Custom ASIC in Three Months", **Mohamed Kassem** of eFabless, at Teardown 2023 (video)

First MPW
Overbooked
45/40

45 designs submitted in 30 days!

All designs must be ***Open Source***



DESIGN TYPES

- 9 x Open processor cores
- 9 x SoC's
- Crypto-currency Miner
- Robotic App Processor
- Amateur Satellite Radio Transceiver
- 7 x Analog/RF
- 5 eFPGA's

COMPANIES

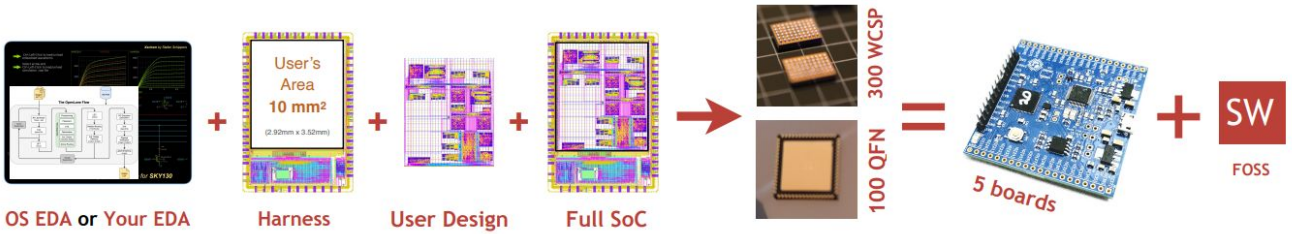
- IBM: OpenPOWER - MicroWatt
- QuickLogic - eFPGA
- Antmicro
- Western Digital - Swerv-EL2
- EFabless
- SpinMemory

efabless.com

"Design and Fund Your Custom ASIC in Three Months", **Mohamed Kassem** of eFabless, at Teardown 2023 (video)

WHAT IS?

chipIgnite
Rapid IC Creation



- Design using SkyWater SKY130 (130nm) rich process + std cells + IO cells
- Start from the Caravel Harness - **no cost** - book your slot for **$200**
- You *choose your licensing terms* for your design - by *default it's proprietary*
- The offered area (10mm2) is not just silicon area - *It is a framed house with plumbing and electricity - just bring your appliances*
- Cycle Time 95 days +/- depending on the package choice

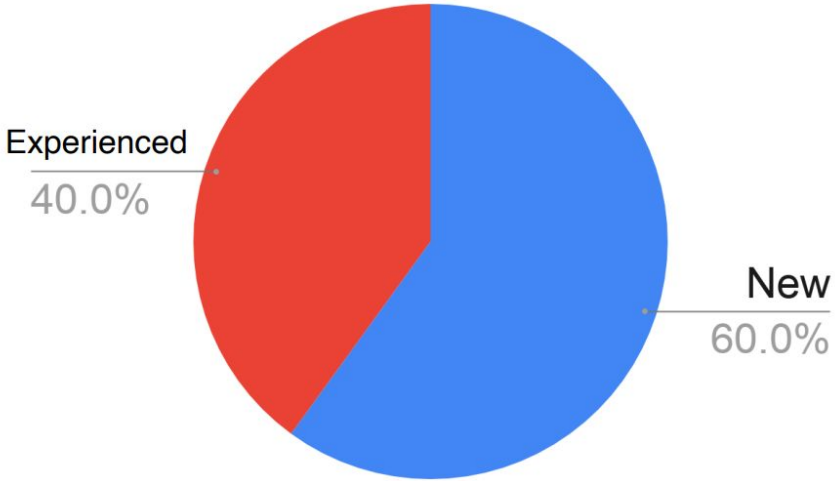
Rapid Prototyping	**$9,750**	**100 QFN**	parts + 5 dev boards
Engineering Samples	**$9,750**	**300 WCSP**	parts + 5 dev boards
Low Volume Production	**$20,000**	1000 WCSP	parts + 5 dev boards

New & Different Type of Users

⅓

self-identity software devs!

60% **first time** designers!



"Design and Fund Your Custom ASIC in Three Months", **Mohamed Kassem** of eFabless, at Teardown 2023 (video)

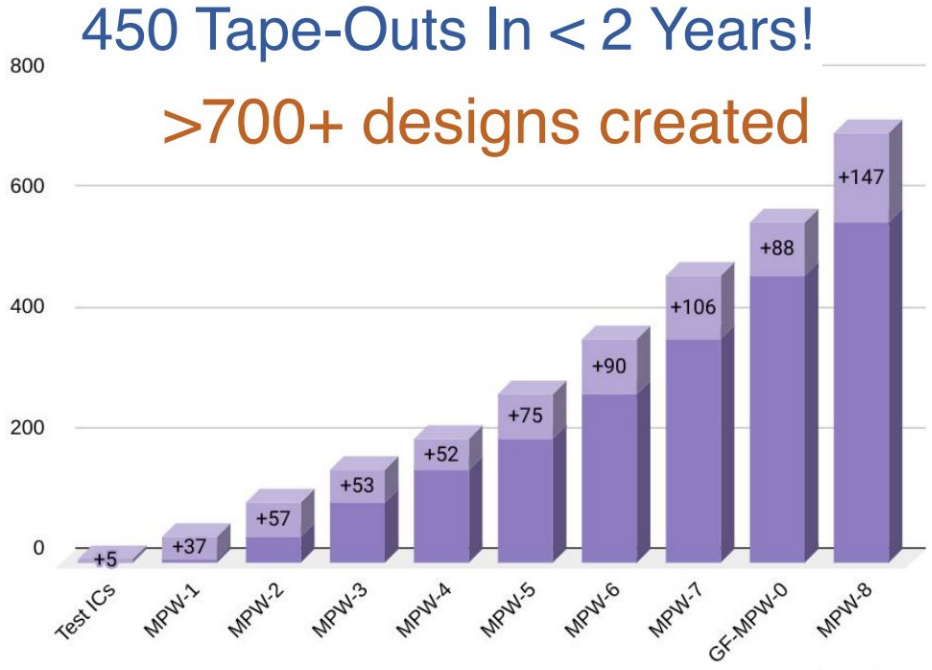
Open Source Designs - Explosive Growth

April 2021 to Date

Fastest Ever *Design Creation Rate*

Sponsored By:

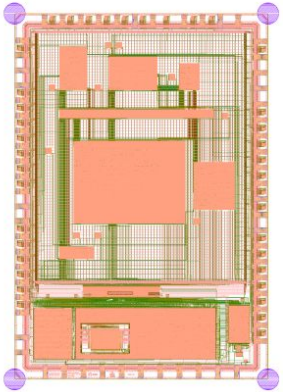
Google

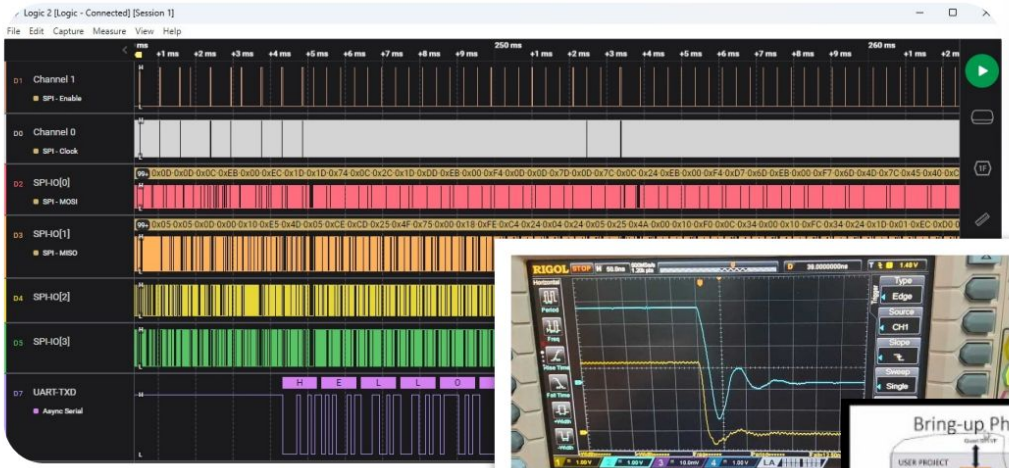


efabless.com

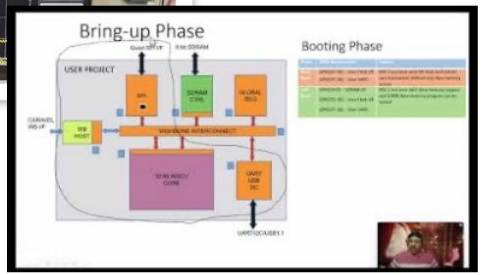
MPW-2 Working Silicon – "Yi-Five"

32-bit RISC-V Core with SDRAM Memory Controller and Quad SPI





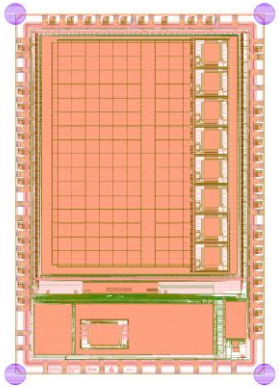
@dineshannayya
SoC designer from Intel



"Being in this VLSI industry for more than 20+ years, I never thought that in my lifetime I would be able to demonstrate my skills from home, develop a 100K+ gate count VLSI design using open source tools, and get it fabricated for free with working silicon. It's a dream come true."

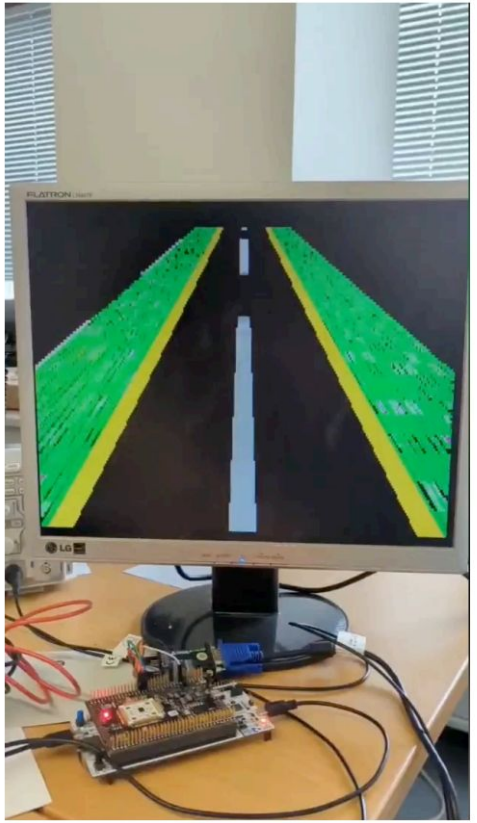
MPW-2 Working Silicon – "FABulous"

Custom FPGA fabric of 896 LUT4s, 64 LUT5s, 8 DSPs and 8KB of BRAMs



"With the MPW2 silicon back and provided harness, we were able to obtain our first silicon results from the FABulous eFPGA fabric generator. This included building a demo that tests all the fabric features - not just LUTs and FFs but also DSPs and BRAM."

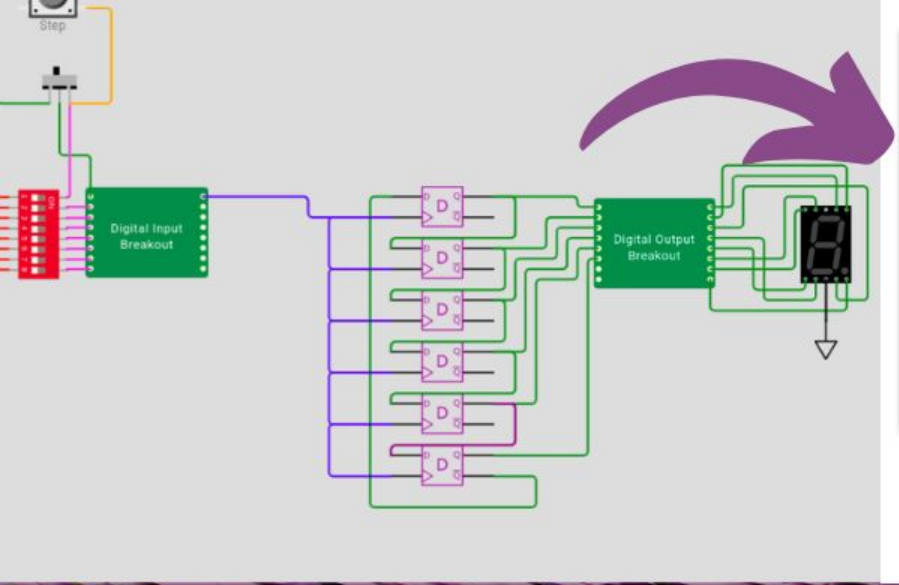
@gatecat
Student at Heidelberg University and FOSS FPGA tool maintainer

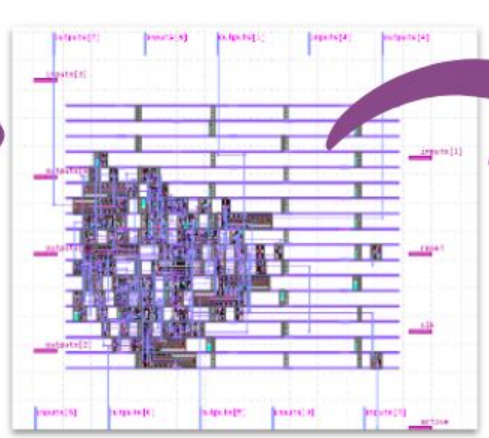


BONUS:

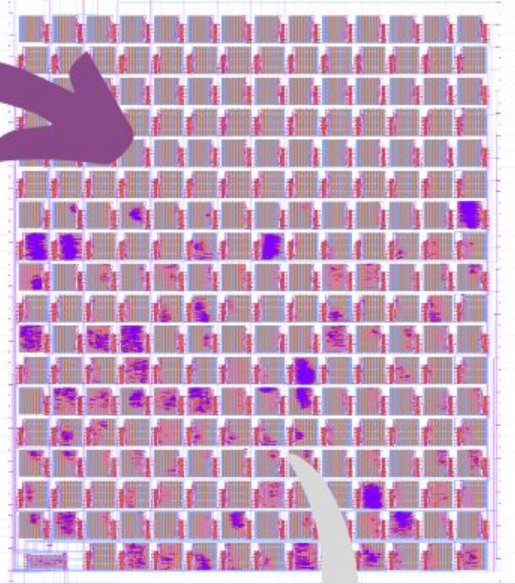
Tiny Tapeout slides from Matt Venn

https://bit.ly/tt-ws-slides



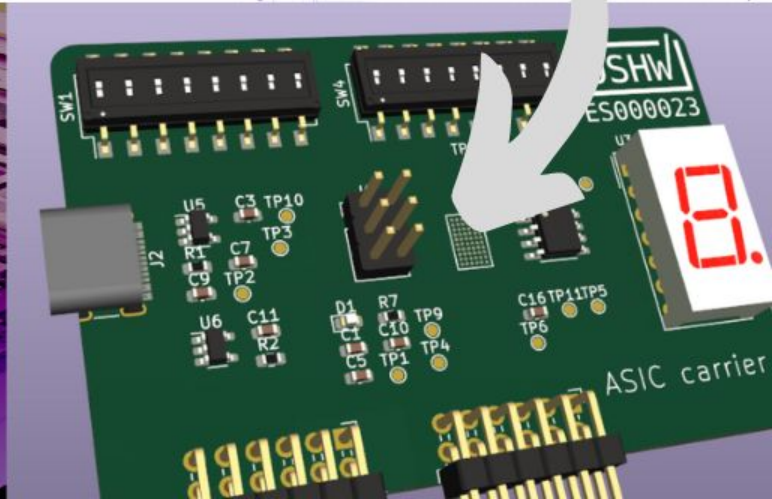


8 bit counter
49 cells

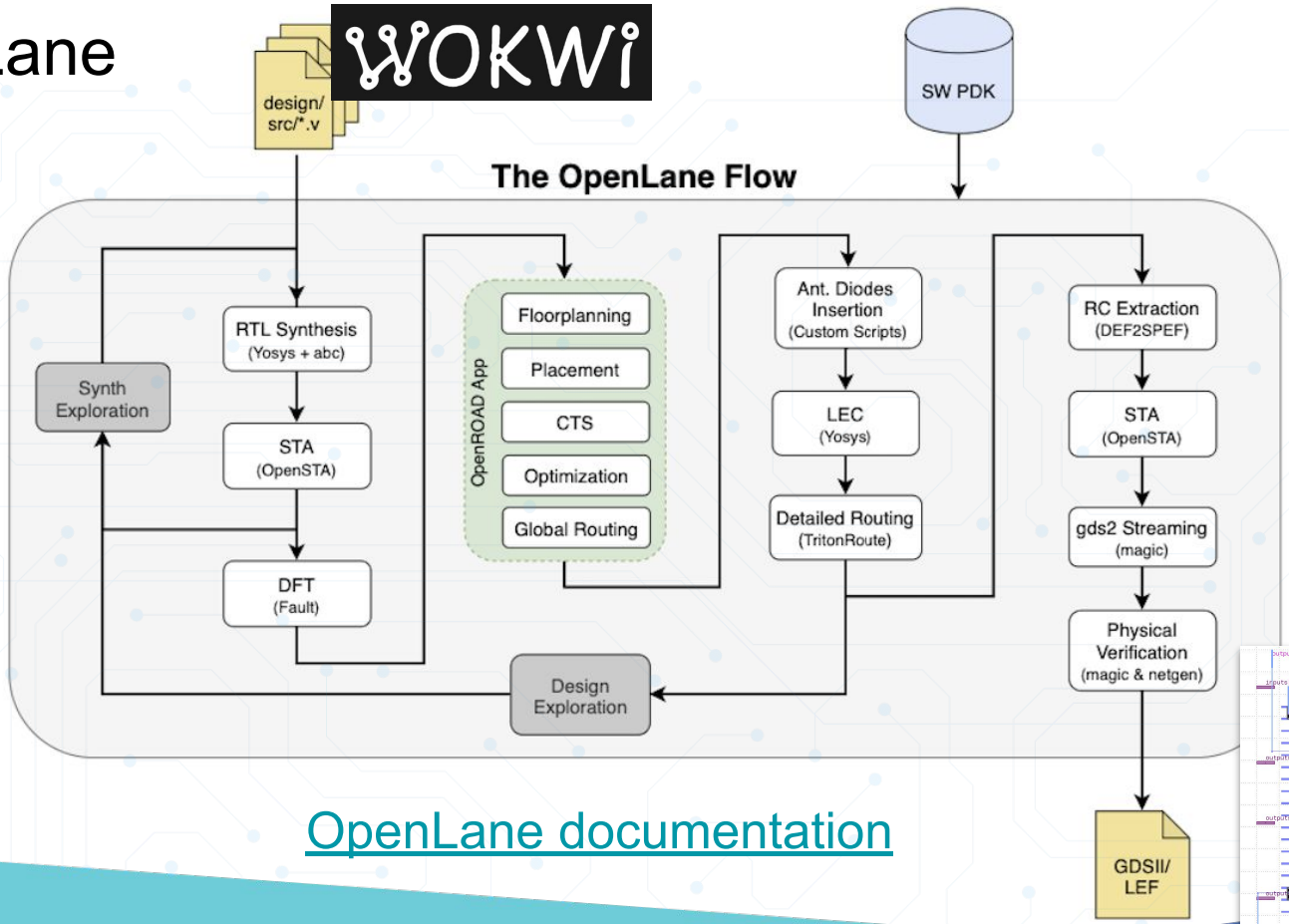


Tiny Tapeout 4

From idea to chip design in minutes!

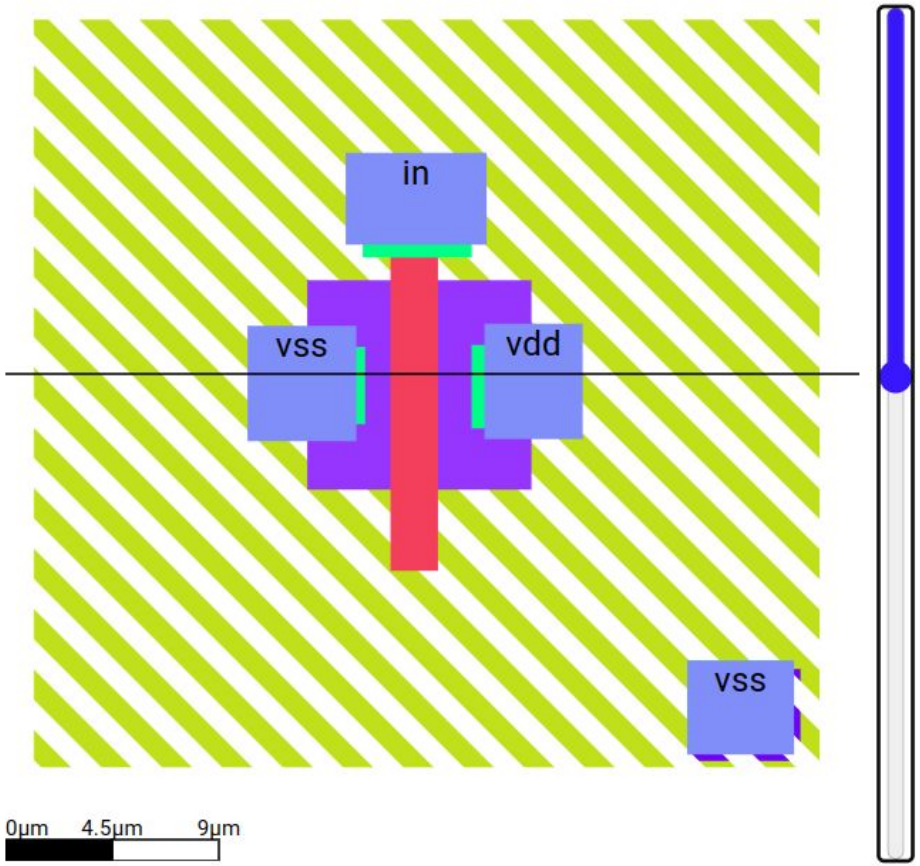


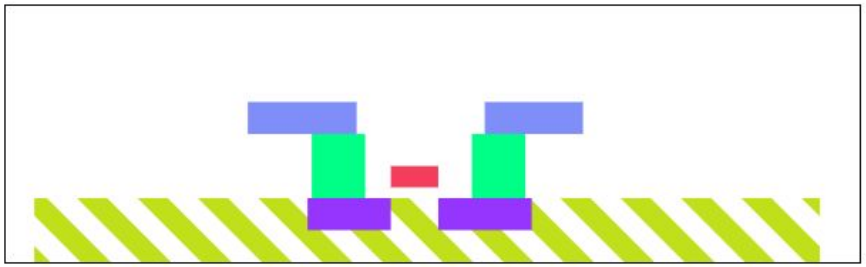
OpenLane



[OpenLane documentation]

Try the interactive version

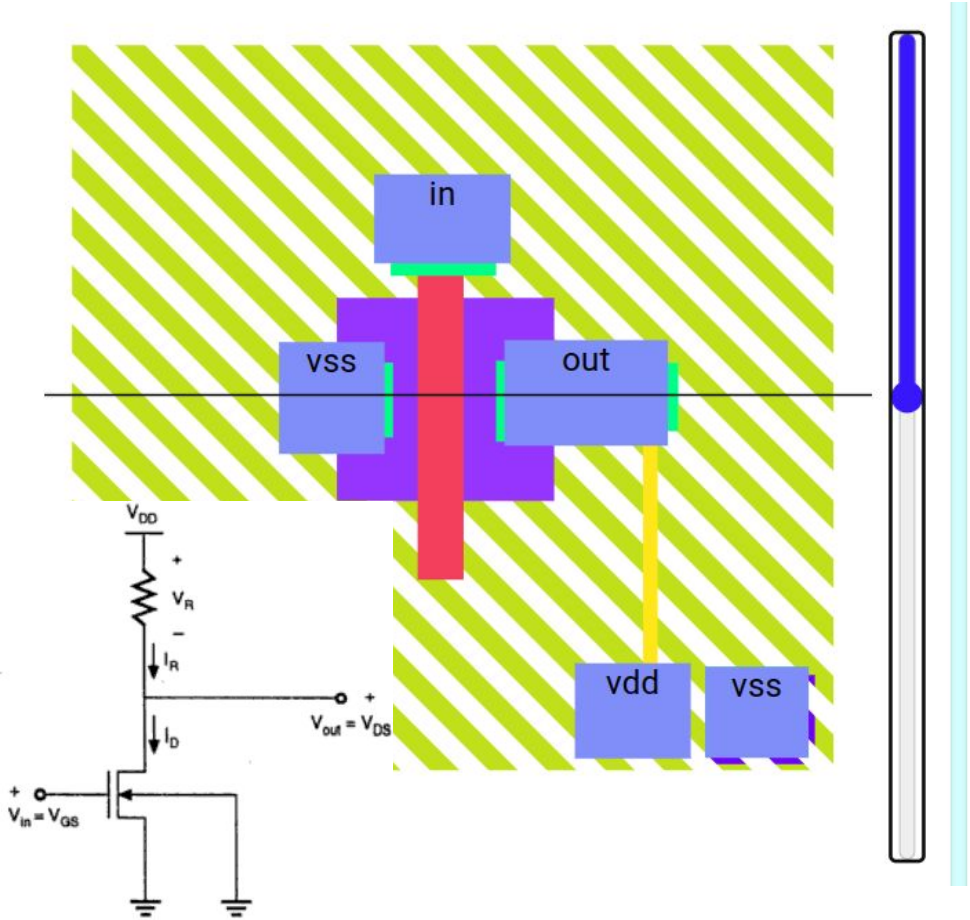


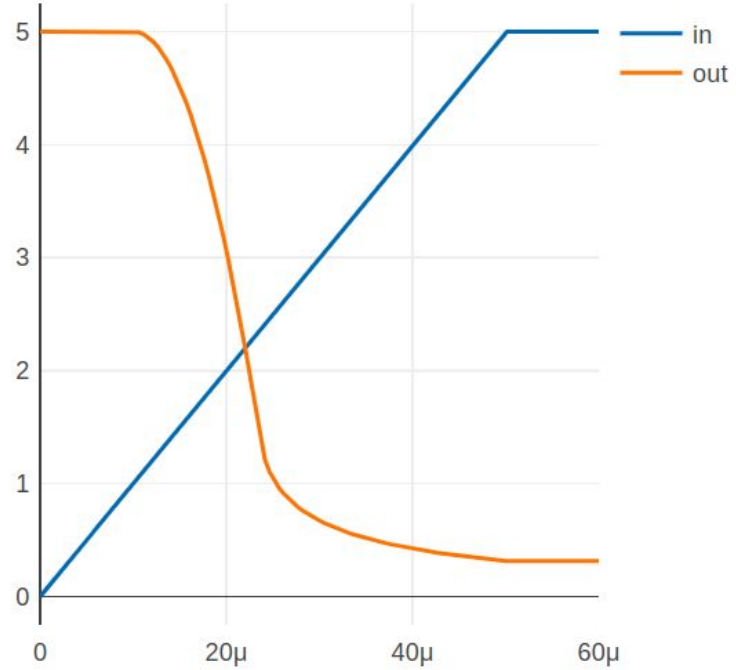


DRC Errors

✅ DRC OK

[Try the interactive version]



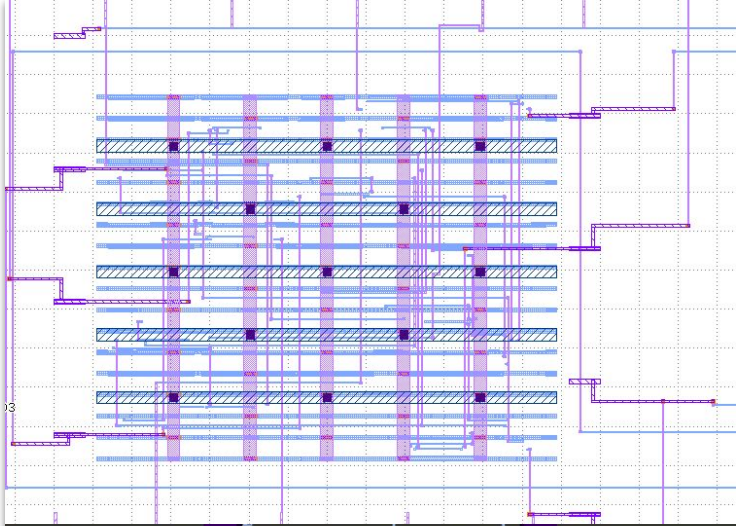


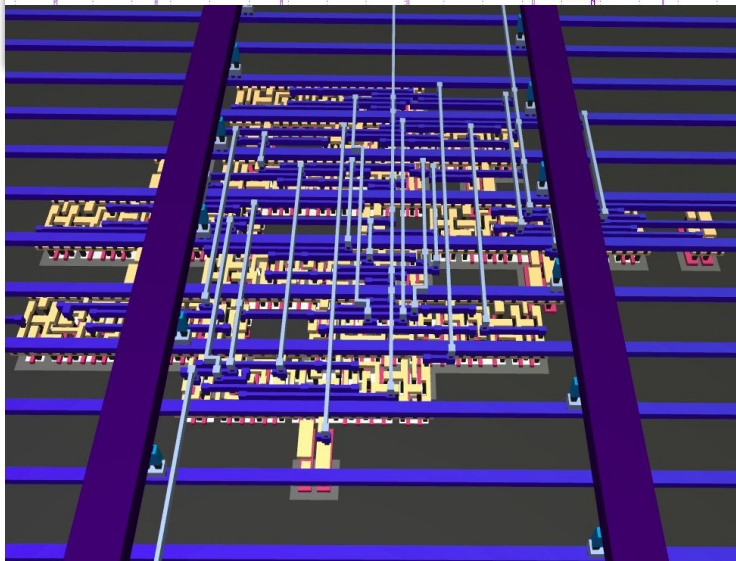
Plot signals:

in ⊗ out ⊗ +

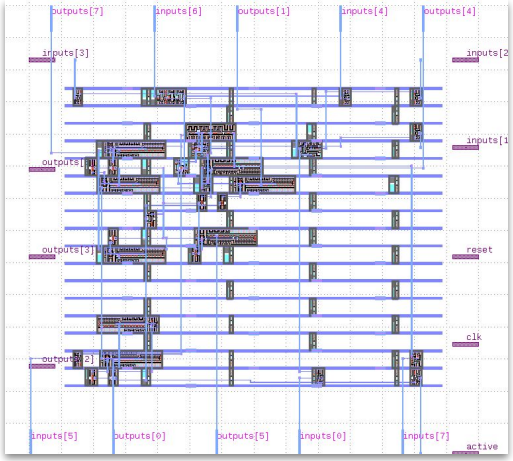
HDL -> GDS

- Create new Github project by forking template
- Update config to fetch your design from Wokwi / use an HDL
- Github action builds the GDS
- 160 x 100 um size
- enough for about 1000 gates
- 10 ins, 8 outs, 8 bidirectional
- No tool install or download
- Easy to share image of your design
- 3D viewer / explorer

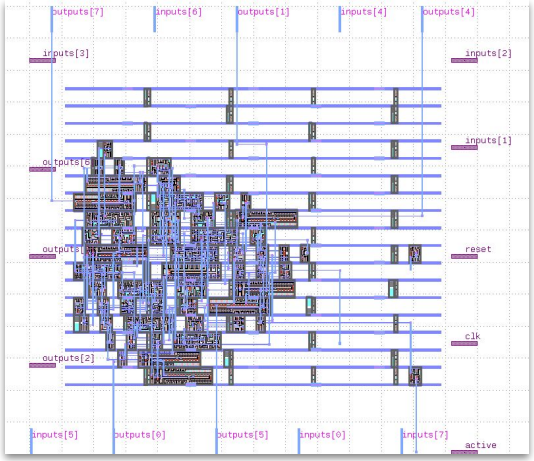




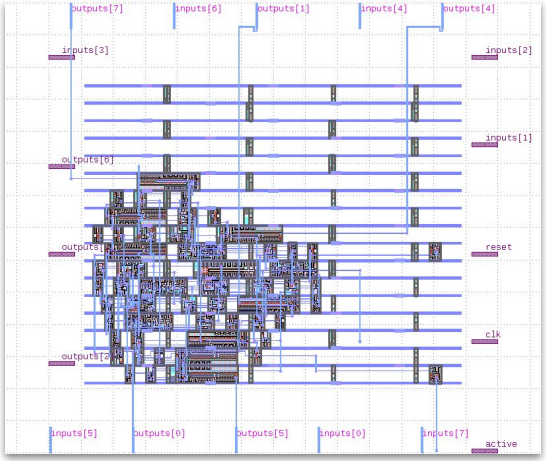
GDS examples (all 70um x 70um)



binary to decimal converter
25 cells



8 bit counter
49 cells



4 bit counter & bcd
50 cells

Optional - pay for your design to be manufactured!

- $100: IC + PCB
- $50: your design on the IC but no chip or PCB

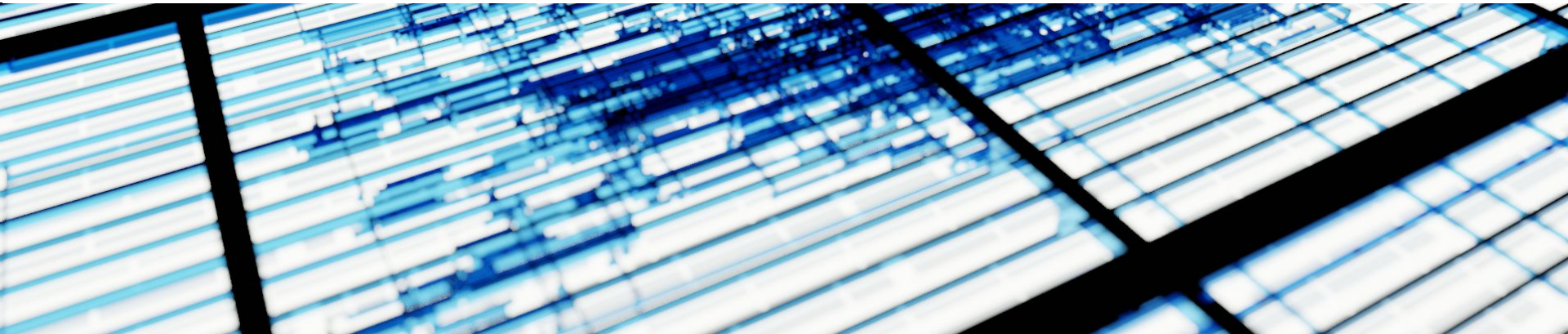
Example School runs workshop for 10 people and orders 1 board:

- 9 x $50 + 1 x $100 = $550
- $550 / 10 participants = **$55 per ticket**

Sponsored by efabless.com

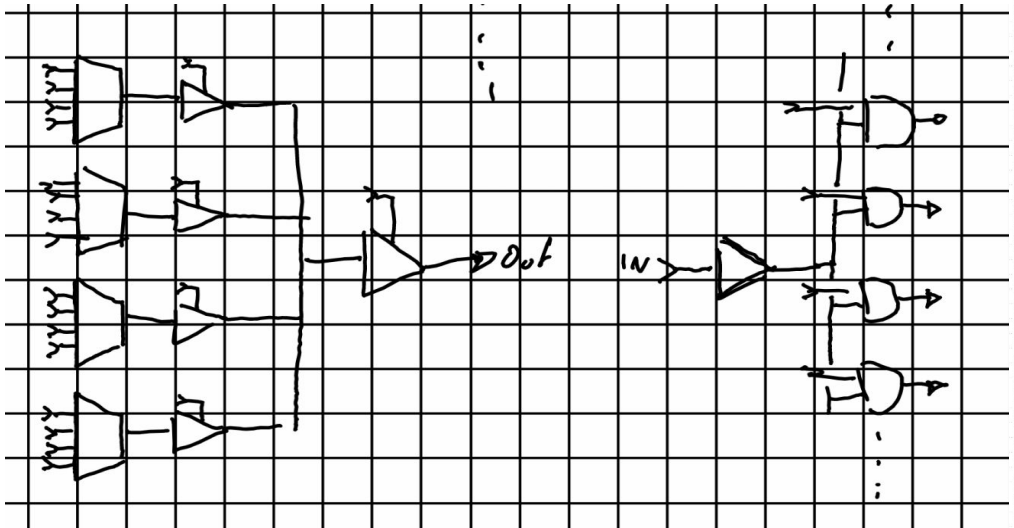
Tiny Tapeout stats

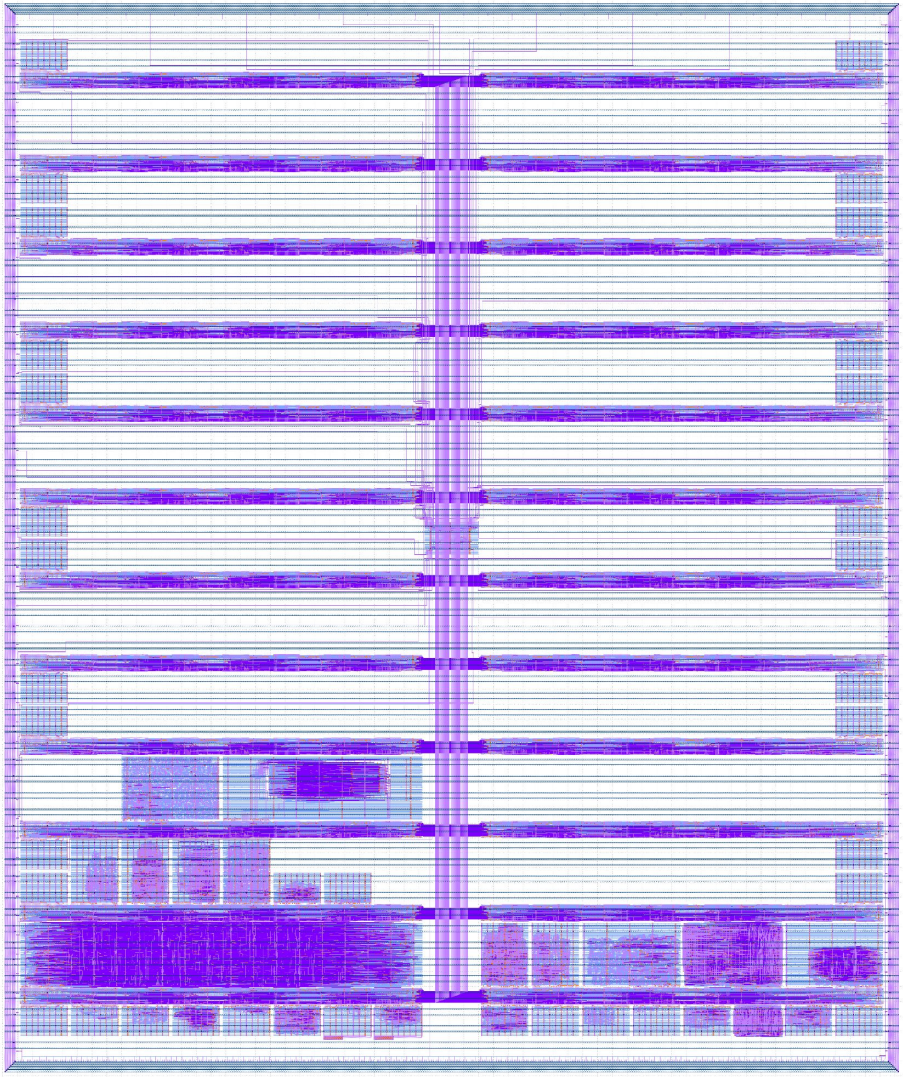
Run	Launched	Closed	Shuttle	Designs
TT01	2022-08-17	2022-09-01	MPW7	152
TT02	2022-11-09	2022-12-02	2211Q	165
TT03	2023-03-01	2023-04-23	2304C	249 (includes 149 from TT02)



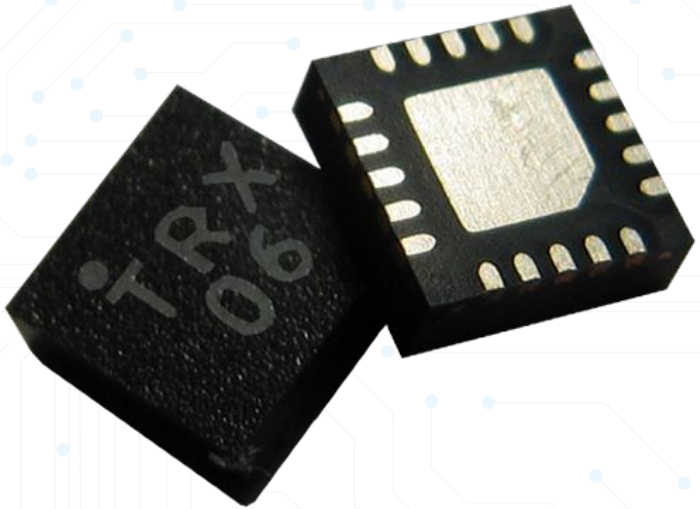
Add new designs

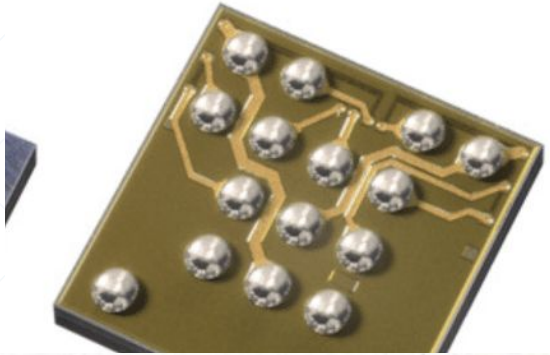
- GDS generation done with GH action
- High speed IO ~50MHz
- Supports around 300 designs
- Multi tile support
- TT04 will tapeout September 202
- [Submission template]

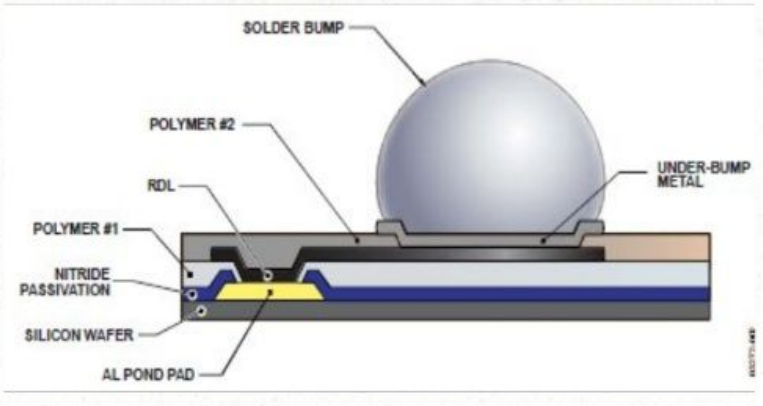




Packaging: QFN or Wafer Level Chip Scale Package

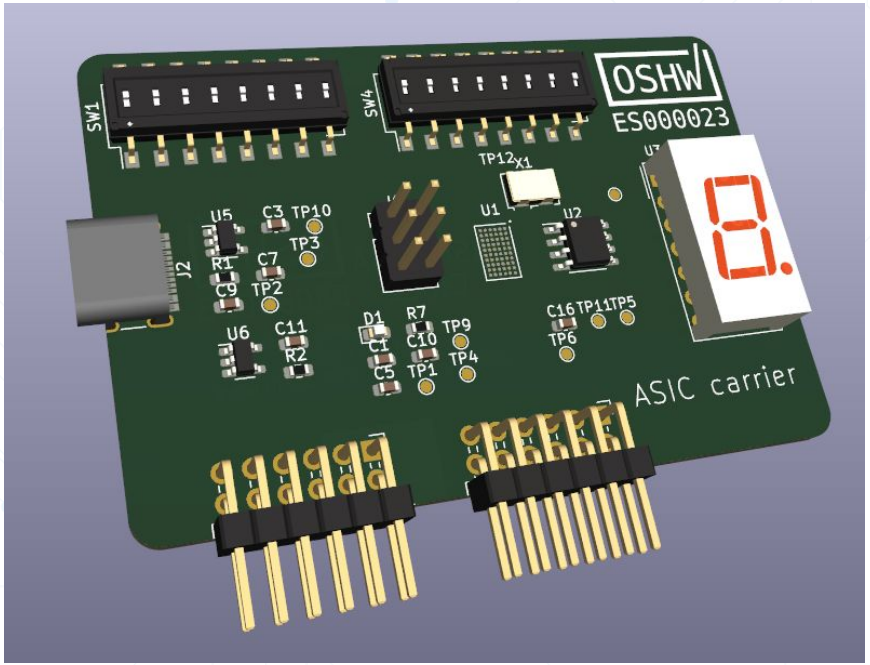






Receive PCB with custom chip mounted

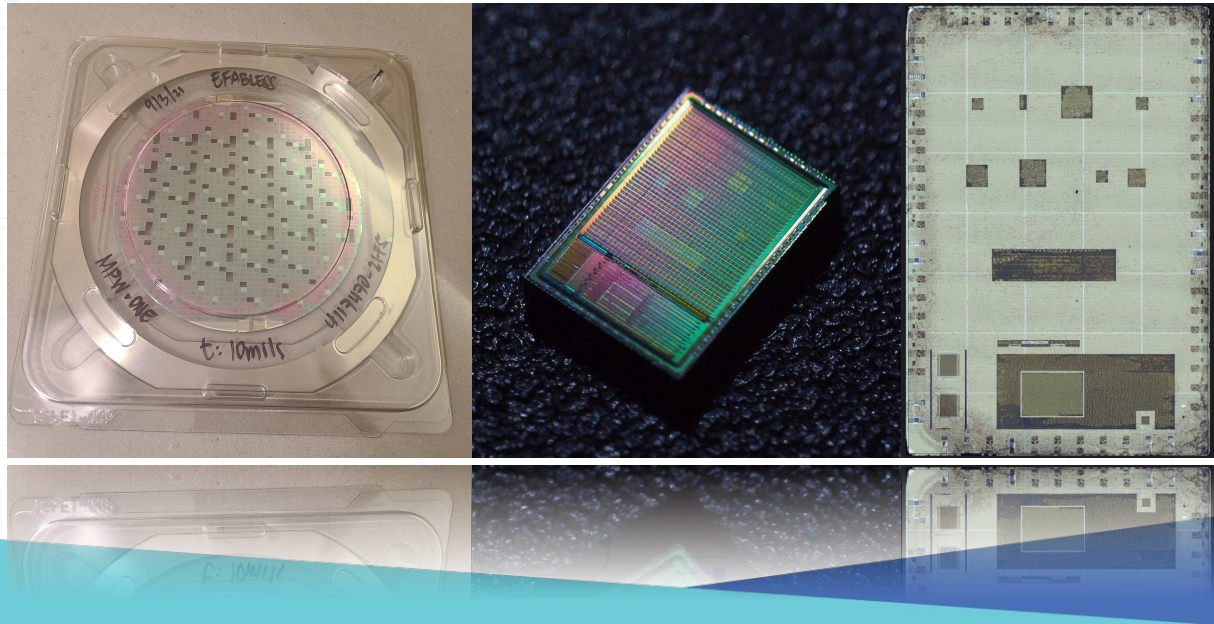
- USB C psu, 3.3v and 1.8v
- Adjustable clock / single step
- 9 dip for design select (or jumpers)
- 8 dip for inputs
- 8 leds for outputs
- Include PMOD headers / mount holes



Mockup

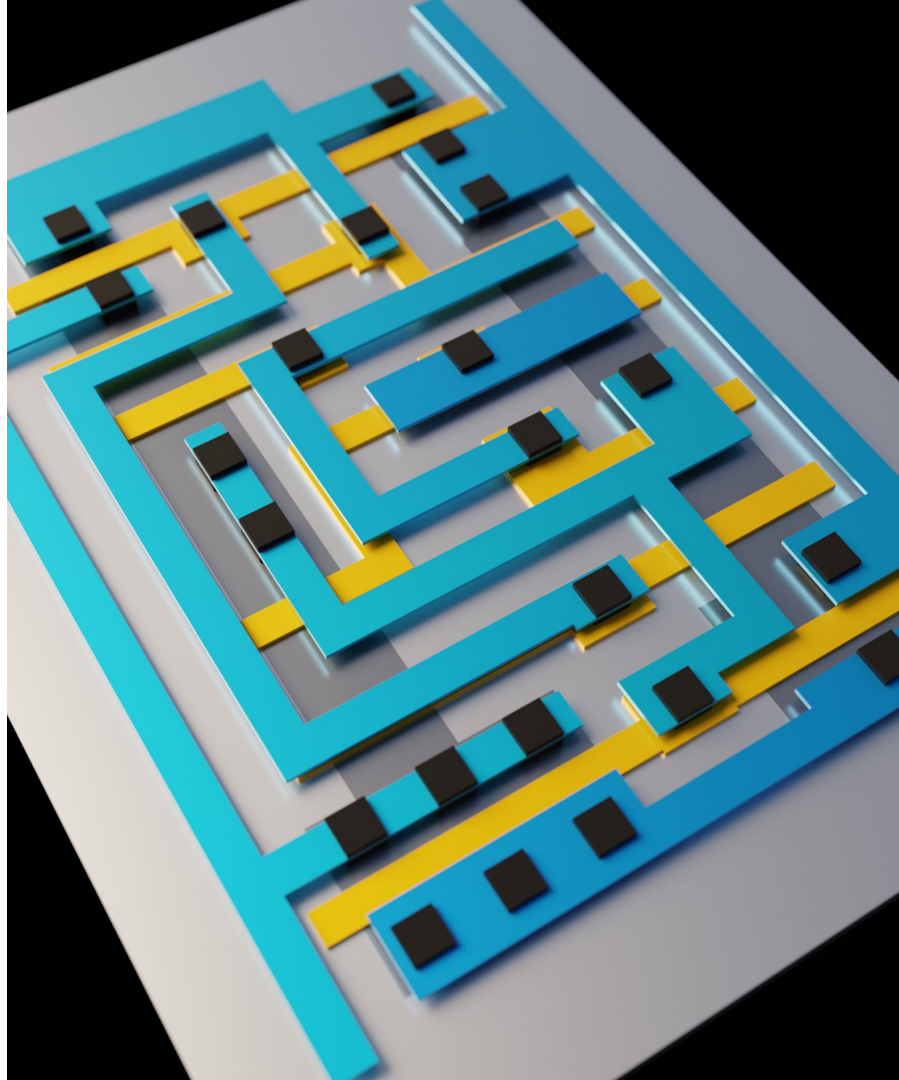
Receive emails throughout the ~6 month wait

- ASIC basics / tutorials / ideas for designs / this week's coolest design
- Virtual factory tour
- Wafers out
- Testing
- PCBs out
- PCBs sent



Connect with me

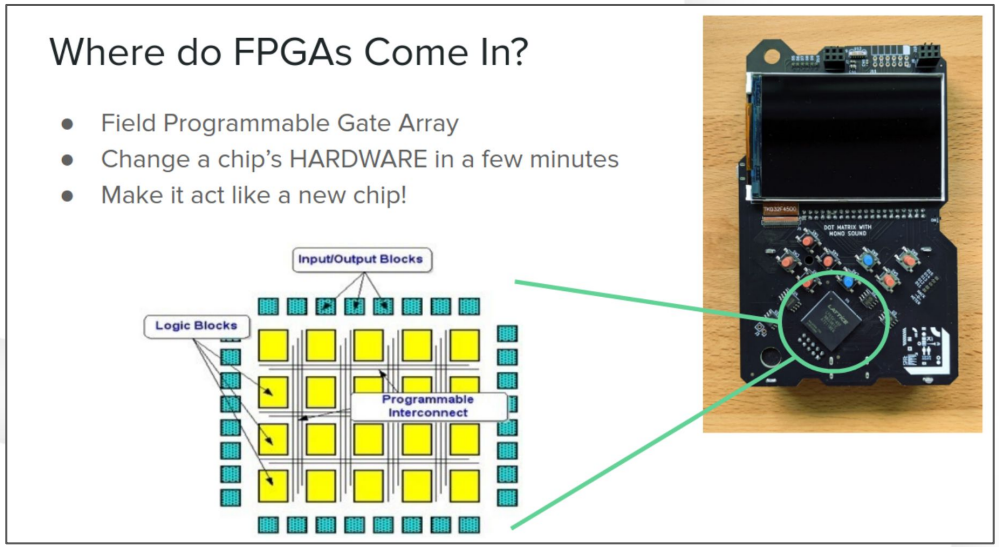
- Slides https://bit.ly/tt-ws-slides
- Newsletter
- Youtube channel
- Twitter @matthewvenn
- Linked.in
- Take my full course



BONUS:
What about RISC-V on FPGAs?

Introduction

- "RISC-V and FPGAs: Open Source Hardware Hacking" keynote at Hackaday Supercon 2019 by Dr. Megan Wachs



Open source FPGA toolchains

- Project IceStorm for Lattice iCE40 FPGA
- Project Trellis for the more capable Lattice ECP5 FPGA
- Project X-Ray for the much more capable Xilinix Series 7
- F4PGA (formerly SymbifFlow):
    - "F4PGA is a fully open source toolchain for the development of FPGAs of multiple vendors. Currently, it targets the Xilinx 7-Series, Lattice iCE40, Lattice ECP5 FPGAs, QuickLogic EOS S3 and is gradually being expanded to provide a comprehensive end-to-end FPGA synthesis flow."

Why design an SoC in Python?

- Python has advantages over traditional HDL like VHDL and Verilog
  - Many people are familiar with Python than HDL (hardware description languages)
- Migen* is a Python framework that helps automate chip design
  - Leverages the object-oriented, modular nature of Python
  - Produces Verilog code so it can be used with existing chip design workflows
  - *Amaranth is the future. Formerly called nMigen which was itself a rewrite of Migen.
  - Myrtle "gatecat" Shah of ChipFlow: Building SoCs with Python and Open Tools

What is Migen?

migen BASICS

```vhdl
-- Libraries imports
library ieee;
use ieee.std_logic_1164.all;

-- Module interface description
entity my_module is
    port(
        clk : in std_logic;
        o   : out std_logic
    );
end entity;

-- Module architecture description
architecture rtl of my_module is
   signal d : std_logic;
   signal q : std_logic;
begin
    -- Combinatorial logic
    o <= q;
    d <= not q;

    -- Synchronous logic
    process(clk)
    begin
        if rising_edge(clk) then
            d <= q
        end if;
    end process

end rtl;
```

VHDL

An alternative HDL based on Python

```python
from migen import *

class MyModule(Module):
    def __init__(self):
        self.o = Signal()

        # # #

        d = Signal()
        q = Signal()

        # combinatorial logic
        self.comb += [
            self.o.eq(q),
            d.eq(~q)
        ]

        # synchronous logic
        self.sync += d.eq(q)
```

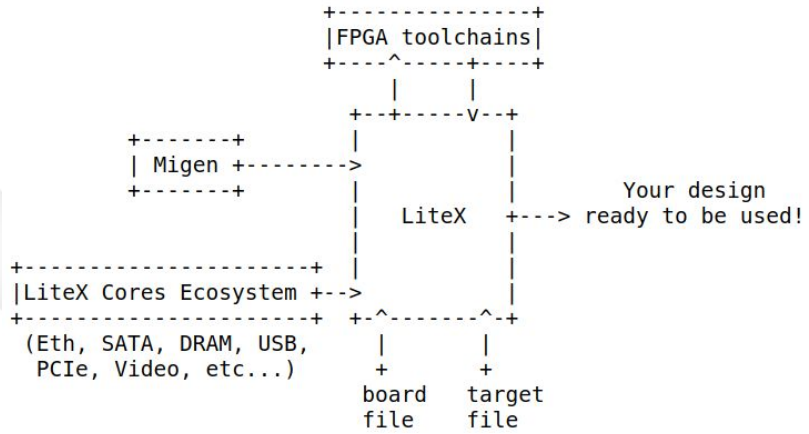
Migen

source: http://goo.gl/mZJvFQ

EnjoyDigital

LiteX

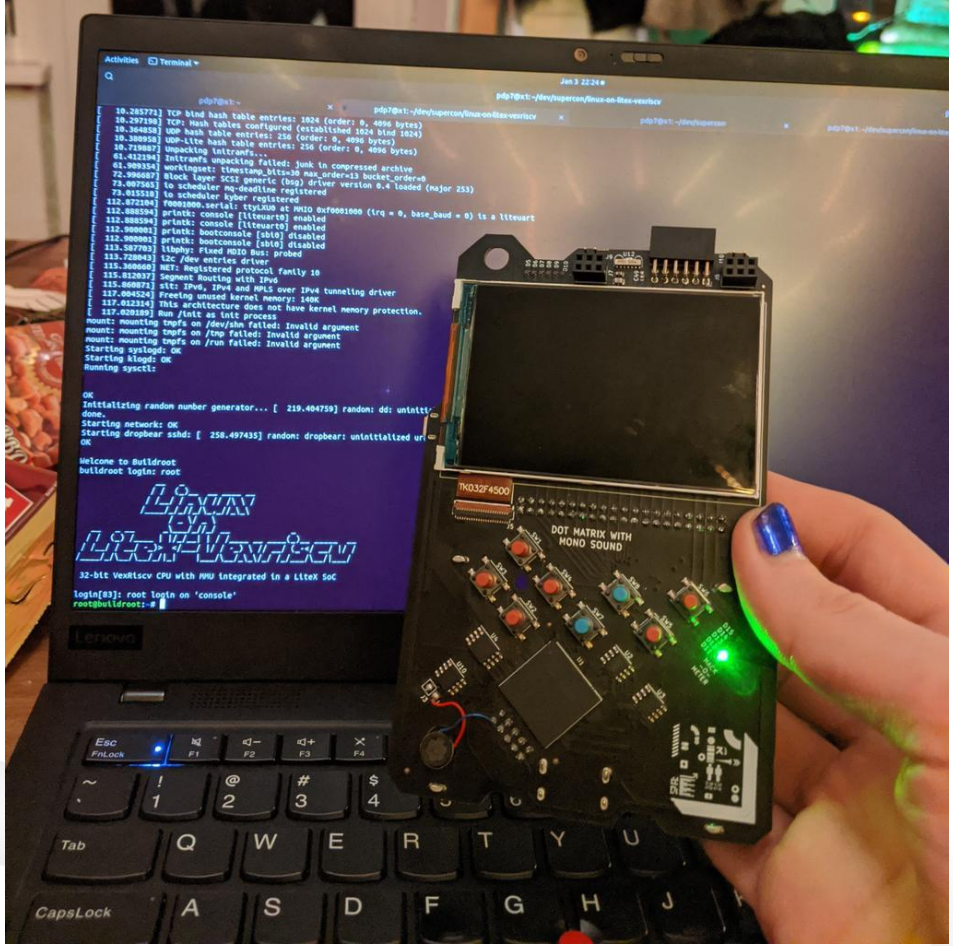
- Based on Migen, builds full SoC that can be loaded into an FPGA
- Collection of open cores for DRAM, Ethernet, PCIe, SATA and more…



Name	Build Status	Description
LiteX-Boards	ci passing	Boards support
LiteDRAM	ci passing	DRAM
LiteEth	ci passing	Ethernet
LitePCIe	ci passing	PCIe
LiteSATA	ci passing	SATA
LiteSDCard	ci passing	SD card
LiteICLink	ci passing	Inter-Chip communication
LiteJESD204B	ci passing	JESD204B
LiteSPI	ci passing	SPI/SPI-Flash
LiteScope	ci passing	Logic analyzer

Linux on LiteX-VexRiscv

- VexRiscv: 32-bit Linux-capable RISC-V core
  - Designed to be FPGA friendly
  - Written in Spinal HDL (based on Scala)
- Builds an SoC using VexRiscv core and LiteX modules
  - Such as LiteDRAM, LiteEth, LiteSDCard, LitePCIe
  - “This project demonstrates how high level HDLs (Spinal HDL, Migen) enable new possibilities and complement each other. Results shown here are the results of a productive collaboration between open-source communities”
- Supports large number of FPGA dev boards including Digilent Arty A7


Activities
Terminal
Welcome to Buildroot
buildroot login: root
Linux on LiteX-VexRiscv
32-bit VexRiscv CPU with MMU integrated in a LiteX SoC
login[83]: root login on 'console'
root@buildroot:~#
TK032F4500
DOT MATRIX WITH MONO SOUND
Lenovo

litex-hub / **litex-boards**

Unwatch 7 | Unstar 17 | Fork 24

Code | Issues 2 | Pull requests 1 | Actions | Projects 0 | Wiki | Security | Insights

add the Hackaday Supercon ECP5 badge #31

Edit

Merged **enjoy-digital** merged 1 commit into `litex-hub:master` from `pdp7:master` 21 days ago

Conversation 18 | Commits 1 | Checks 1 | Files changed 2 | +461 −0

pdp7 commented 22 days ago • edited — Contributor

Add the Hackaday Supercon 2019 badge which has an ECP5 FPGA.

These changes are from a fork by Michael Welling (**@mwelling**)

During Supercon, we tried two approaches:

- use the built-in 16MB QSPI SRAM
- use add-on cartiridge with 32MB SDRAM by Jacob Creedon

We were not able to get the QSPI SRAM working so I've removed those changes, and I have just added the changes that are needed to boot Linux with the 32MB SDRAM.

In addition to **@mwelling**, thank you to Jacob Creedon (**@jcreedon**), **@gregdavill**, Tim Ansell (**@mithro**), and Sean Cross (**@xobs**) who all helped get Linux working on this badge.

KiCad design files by **@jcreedon** for the SDRAM cartridge are available on GitHub.

Reviewers
No reviews

Assignees
No one assigned

Labels
None yet

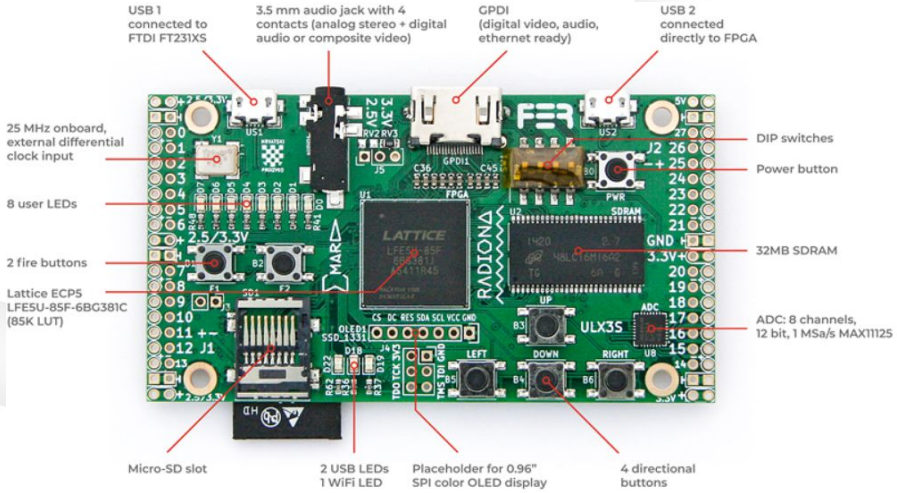
Projects
None yet

Milestone
No milestone

Open Source ECP5 FPGA boards

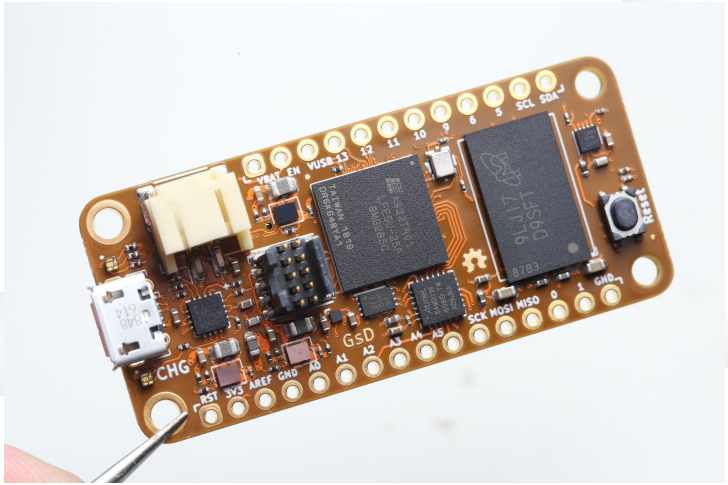
- [Radiona.org ULX3S]

  - 32MB SDRAM; ESP32 on-board for WiFi and Bluetooth; $115 on [CrowdSupply] or [Mouser]



Open Source ECP5 FPGA boards

- OrangeCrab by Greg Davill
  - 128MB DDR RAM; Adafruit Feather form factor; available for $129



Want to learn FPGAs? Try Fomu!

- Online workshop from Tim Ansell and Sean Cross
- $50 on CrowdSupply
- Fits inside USB port!
- Learn how to use:
  - MicroPython
  - Verilog
  - LiteX