User's Manual

R-Car H3 / M3

User's Manual: Hardware

SoCs for Automotive Information Terminal Applications

arm

R-Car Family / R-Car Gen3 Series

— Preliminary —

Supplement information for Video Signal Processor (VSP2)

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

32. Video Signal Processor (VSP2)

R-Car H3
R-Car M3

32.1 Overview

The VSP2 is the successor IP of Renesas' VSP-IP series which supports image processing such as super resolution, sharpness, up/down scaling, 1D look-up tables, 3D look-up tables, histogram, image blending, rotation/flipping, interface to Display Unit (DU) and Display Output Compare (DISCOM).

Description of Display Output Compare (DISCOM) is shown in the section 32.5.

32.1.1 Features

This LSI incorporates different types of VSP2 modules (VSPI, VSPBS, VSPBC, VSPBD, VSPB, VSPD and VSPDL) as image processing systems. Table 32.1 shows the number of VSP for each product.

The VSPI supports image processing by memory to memory such as super resolution, sharpness, up/down scaling, look-up tables, histogram and rotation/flipping. [R-Car H3/ /R-Car M3]

The VSPBC supports image processing by memory to memory such as look-up tables, 1D-histogram and image blending. [R-Car H3].

The VSPBD supports image processing by memory to memory such as image blending [R-Car H3].

The VSPB supports image processing by memory to memory such as look-up tables, 1D-histogram, image blending and vertical flipping, VSPB is composed by unifying VSPBC function with VSPBD function for R-Car M3. [R-Car M3]

The VSPD supports image processing such as image blending, interface to Display Output Compare (DISCOM) and output image data to Display Unit (DU) with or without writing back the image data to memory. The VSPD supports image processing by memory to memory also, but the VSPD cannot output image data to Display Unit (DU) in that case. [R-Car H3 /R-Car M3]

The VSPDL supports image processing such as image blending, Display Output Compare (DISCOM) and output image data to Display Unit (DU) with or without writing back the image data to memory. The VSPDL supports two interfaces with Display Unit (DU). The VSPDL supports image processing by memory to memory also, but the VSPDL cannot output image data to Display Unit (DU) in that case. [R-Car H3]

Table 32.1 VSP2 configuration

Module Name	Number of channels	
	R-Car H3	R-Car M3
VSPI	2	1
VSPBC	1	0
VSPBD	1	0
VSPB (*)	0	1
VSPBS	0	0
VSPD	2	3
VSPDL	1	0

Note: *
Each VSPs features are shown in from section 32.1.1.1 to section 32.1.1.6.

32.1.1.1 Features of VSPI [R-Car H3 /R-Car M3]

- Supports various data formats and conversion
  - Supports YCbCr444/422/420, RGB, α RGB, α plane.
  - Color space conversion and changes to the number of colors by dithering
  - Color keying
  - Supports combination between pixel alpha and global alpha.
  - Supports generating pre multiplied alpha.
- Video processing
  - Supporting 4K (3840 pixels × 2160 lines) [R-Car H3/ R-Car M3]
  - Up and down scaling with arbitrary scaling ratio
  - Super resolution processing
  - Sharpness filter
  - 1D look up table
  - 3D look up table
  - Supports Hue, brightness, and saturation format for look up table or/and histogram.
  - 1D histogram
  - 2D histogram
  - Image rotation with unit of 90-degree, vertical and horizontal flipping

32.1.1.2 Features of VSPBD [R-Car H3]

- Supports various data formats and conversion
  - Supports YCbCr444/422/420, RGB, α RGB, α plane.
  - Color space conversion and changes to the number of colors by dithering
  - Color keying
  - Supports combination between pixel alpha and global alpha.
  - Supports generating pre multiplied alpha.
- Video processing.
  - Supporting 4K (3840 pixels × 2160 lines)
  - Blending of five picture layers and raster operations (ROPs)
  - Vertical flipping

32.1.1.3 Features of VSPBC [R-Car H3]

- Supports various data formats and conversion
  - Supports YCbCr444/422/420, RGB, α RGB, α plane.
  - Color space conversion and changes to the number of colors by dithering
  - Color keying
  - Supports combination between pixel alpha and global alpha.
  - Supports generating pre multiplied alpha.
- Video processing
  - Supporting 4K (3840 pixels × 2160 lines)
  - Blending of five picture layers and raster operations (ROPs)
  - 1D look up table
  - 3D look up table
  - 1D histogram
  - Vertical flipping

32.1.1.4 Features of VSPB [R-Car M3]

- Supports various data formats and conversion
  - Supports YCbCr444/422/420, RGB, α RGB, α plane.
  - Color space conversion and changes to the number of colors by dithering
  - Color keying
  - Supports combination between pixel alpha and global alpha.
  - Supports generating pre multiplied alpha.
- Video processing
  - Supporting 4K (3840 pixels × 2160 lines) [R-Car M3]
  - Blending of five picture layers and raster operations (ROPs)
  - 1D look up table
  - 3D look up table
  - 1D histogram
  - Vertical flipping

32.1.1.5 Features of VSPD

- Supports various data formats and conversion
  - Supports YCbCr444/422/420, RGB, α RGB, α plane.
  - Color space conversion and changes to the number of colors by dithering
  - Color keying
  - Supports combination between pixel alpha and global alpha.
  - Supports generating pre multiplied alpha.
- Video processing
  - Blending of five picture layers and raster operations (ROPs)
  - Vertical flipping in case of output to memory.
- Direct connection to display module
  - Supporting 4096 pixels in horizontal direction [R-Car H3 /R-Car M3]
  - Writing back image data which is transferred to Display Unit (DU) to memory.
- Supports DISCOM function.

32.1.1.6 Features of VSPDL [R-Car H3]

- Supports various data formats and conversion
  - Supports YCbCr444/422/420, RGB, α RGB, α plane.
  - Color space conversion and changes to the number of colors by dithering
  - Color keying
  - Supports combination between pixel alpha and global alpha.
  - Supports generating pre multiplied alpha.
- Video processing
  - Blending of five picture layers and raster operations (ROPs)
  - Vertical flipping in case of output to memory.
- Direct connection to display module
  - Supporting two display output interfaces
  - Supporting 2048 pixels in horizontal direction.
  - Writing back image data which is transferred to Display Unit (DU) to memory.
- Supports DISCOM function.

32.1.2 Block diagram

32.1.2.1 Block diagram of each VSP

Figure 32.1 to Figure 32.8 shows the configuration of VSPI, VSPBC, VSPBD, VSPB, VSPBS, VSPD and VSPDL sub modules.

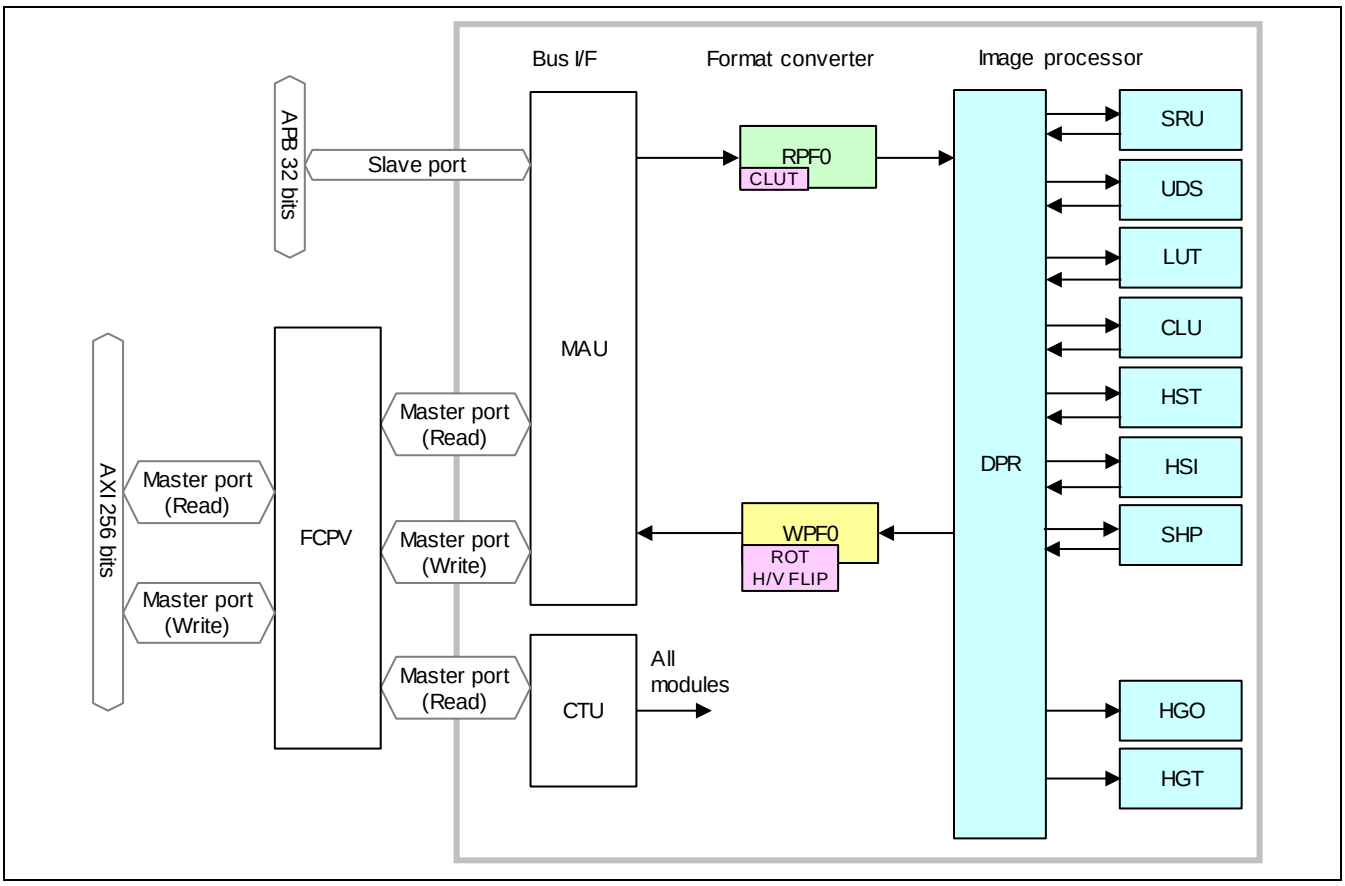


Figure 32.1 VSPI Module Configuration
[R-Car H3/ R-Car M3]

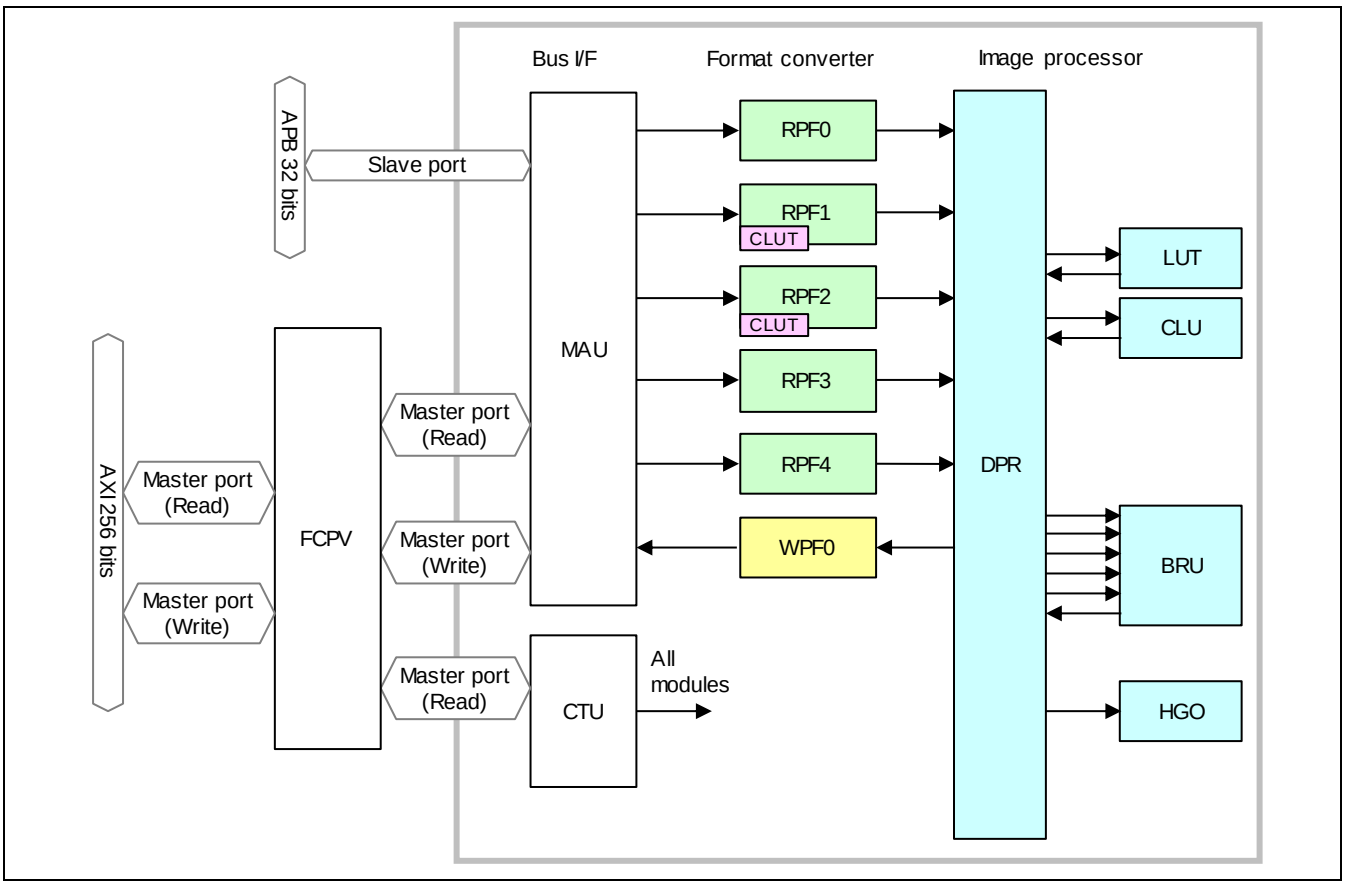


Figure 32.2 VSPBC Module Configuration [R-Car H3]

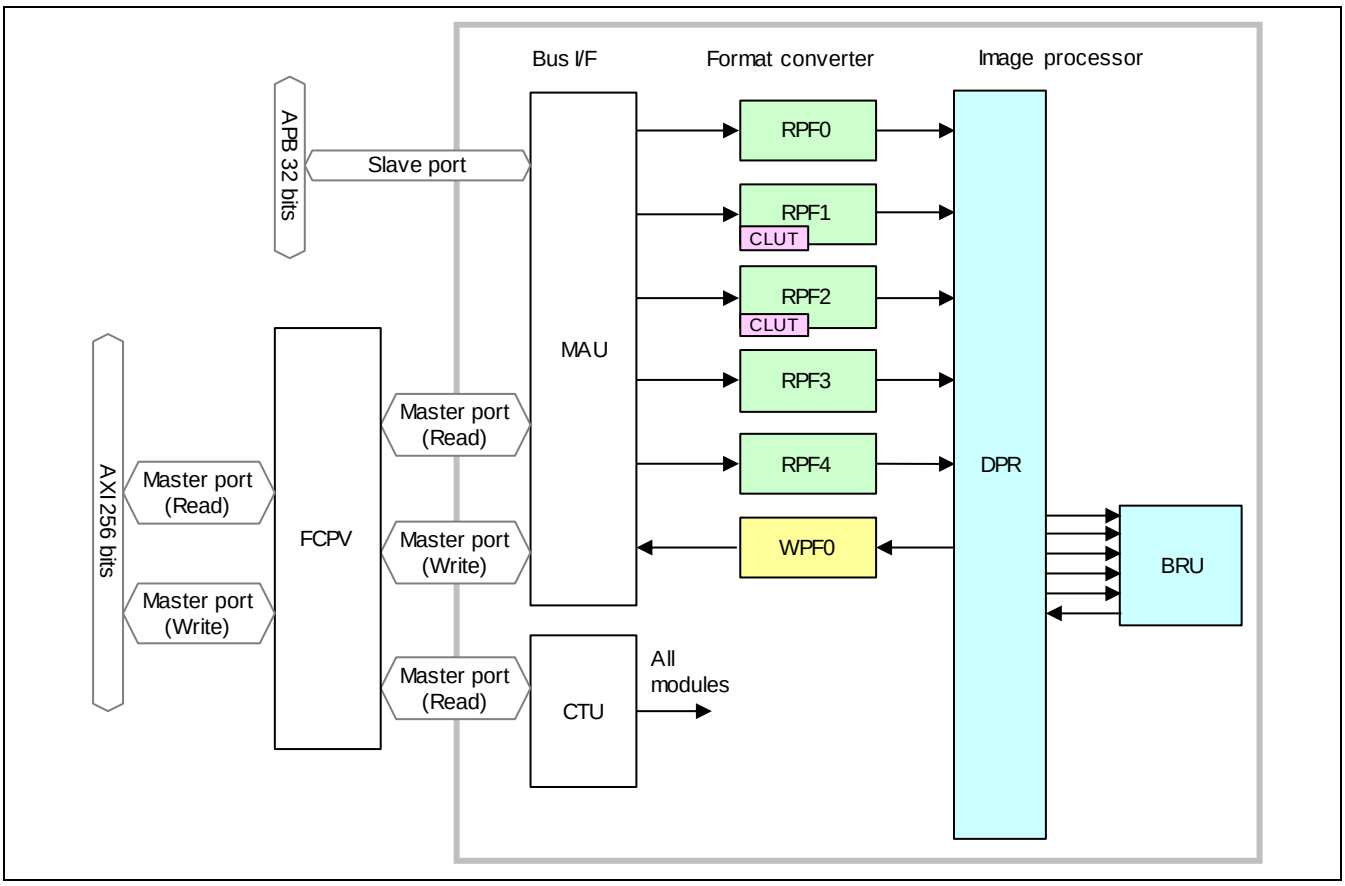


Figure 32.3 VSPBD Module Configuration [R-Car H3]

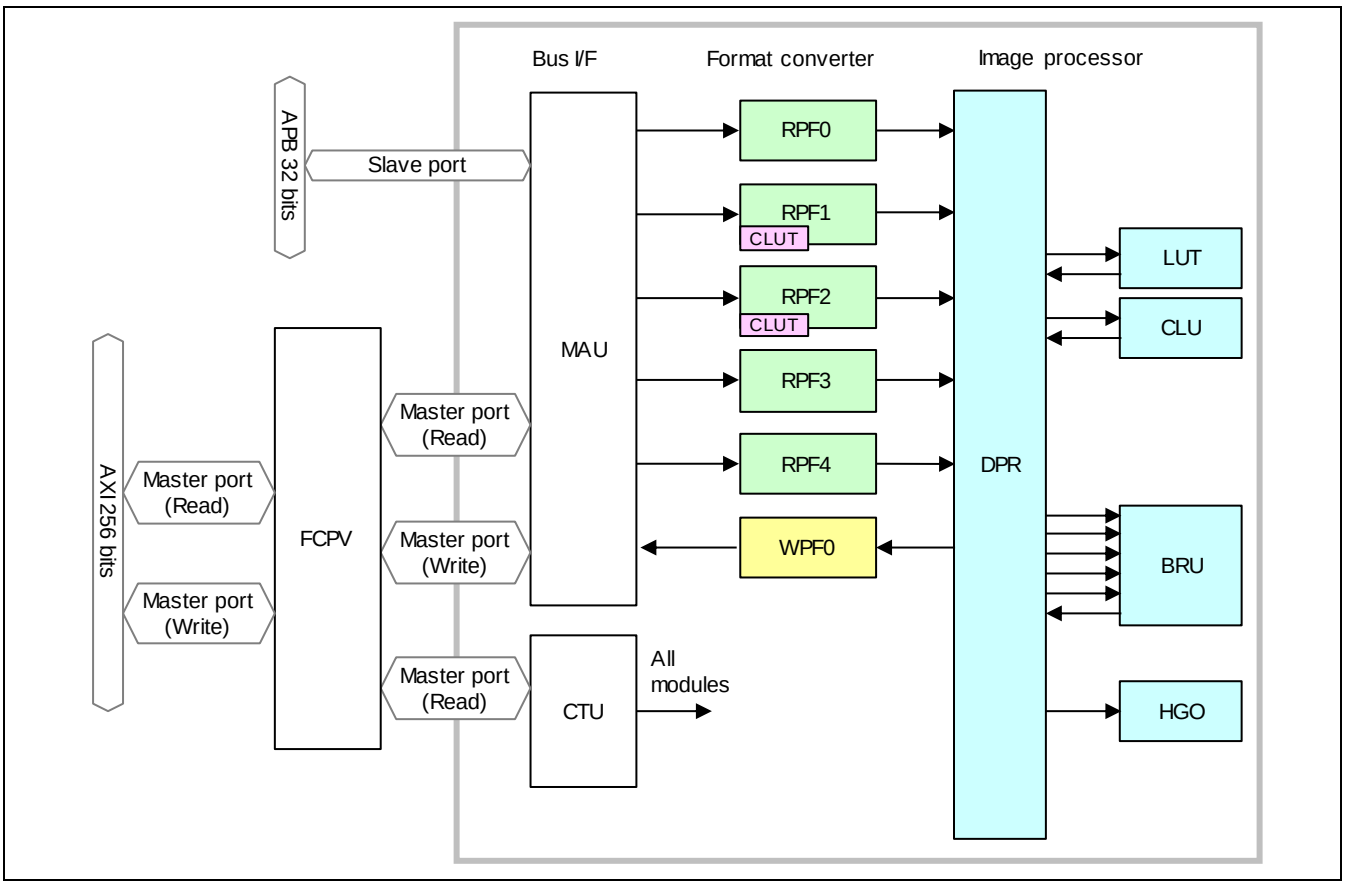
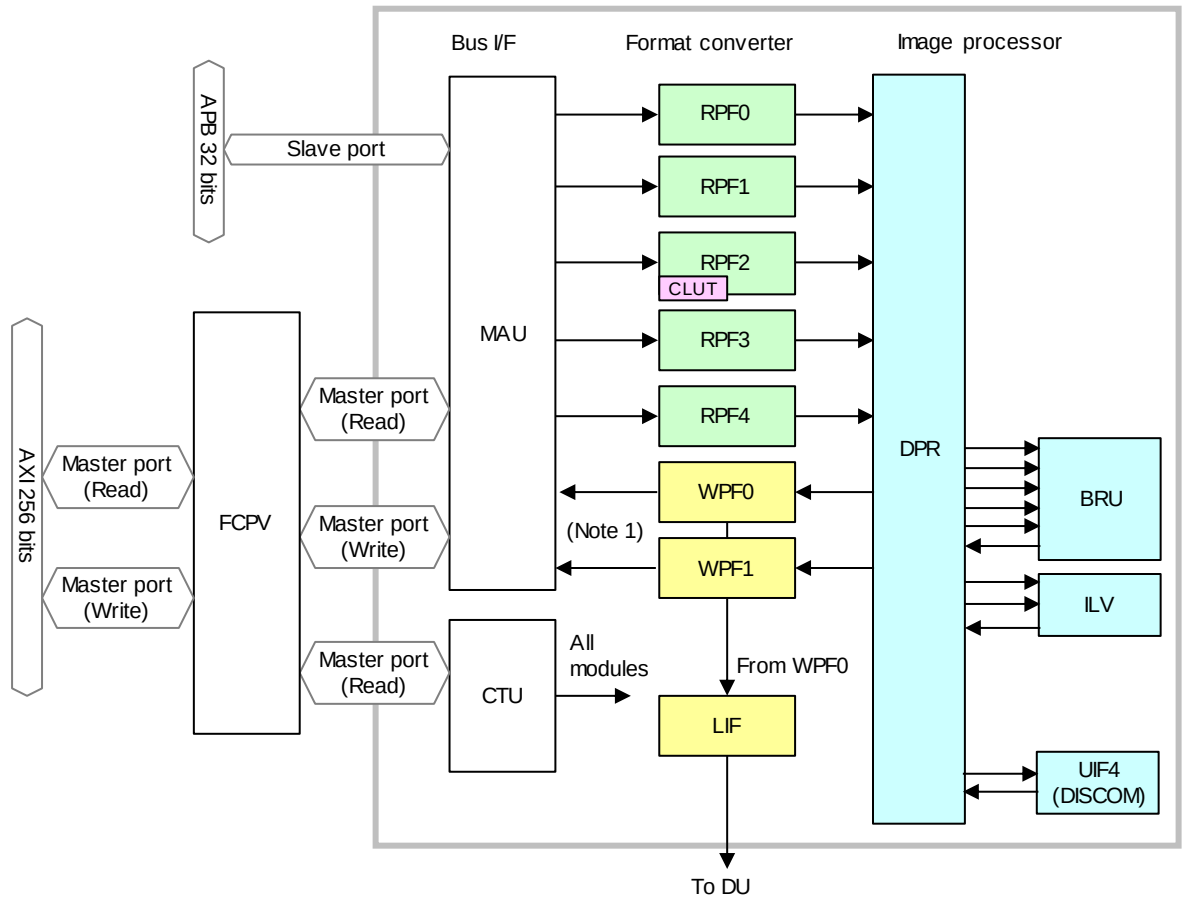


Figure 32.4 VSPB Module Configuration [R-Car M3]



(Note1) WPF0 and WPF1 cannot be executed in parallel. Three following cases are available.

- Activating WPF0 for transferring image data to Display Unit (DU)
- Activating WPF0 for transferring image data to Display Unit (DU), and writing back the image data to memory.
- Activating WPF1 for memory to memory processing.

Figure 32.6 VSPD Module Configuration
[R-Car H3 /R-Car M3]

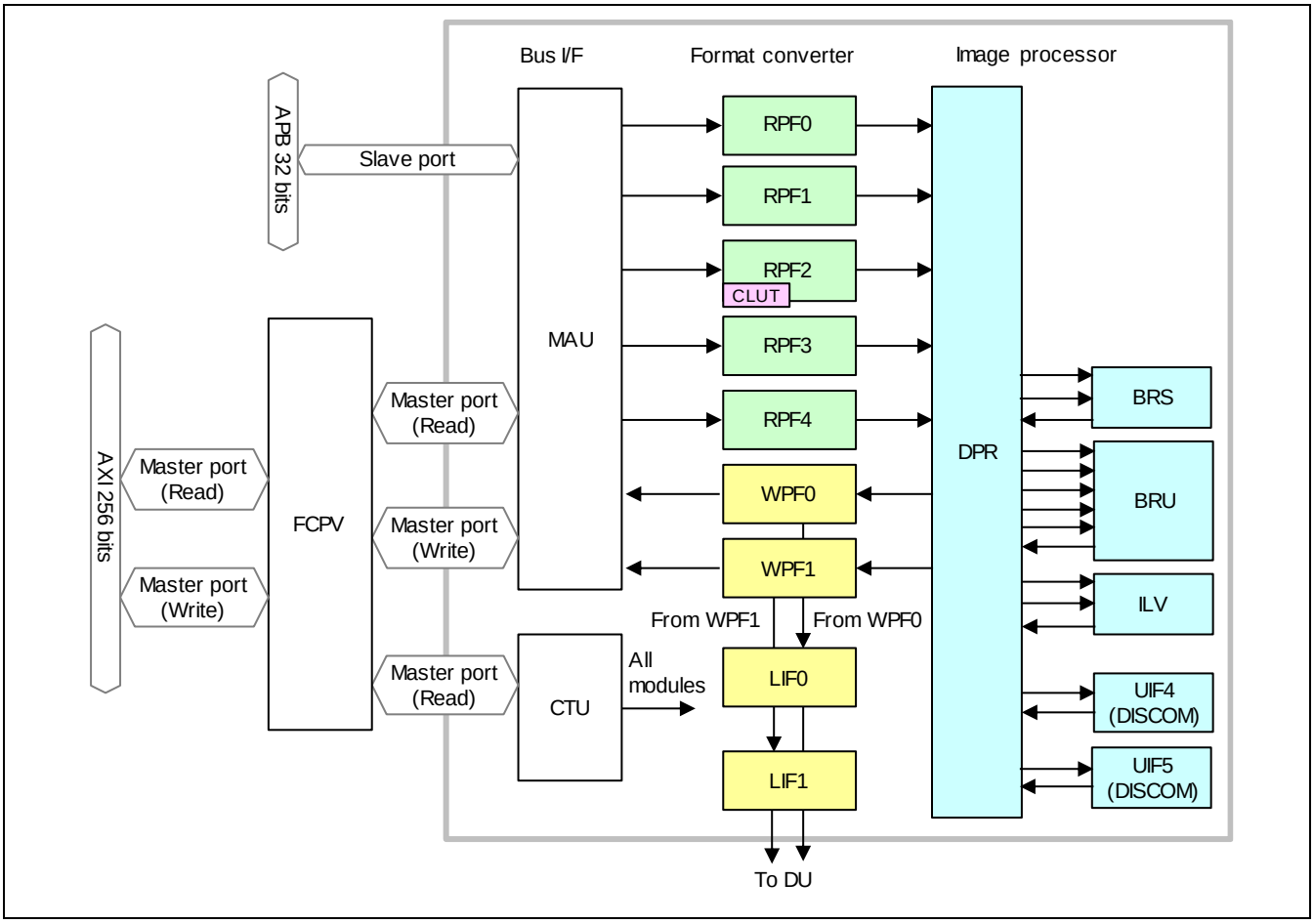


Figure 32.8 VSPDL Module Configuration [R-Car H3]

Memory Access Unit (MAU)

Command Transfer Unit (CTU)

Read Pixel Formatter (RPF)

Data Path Router (DPR)

Super Resolution Unit (SRU)

Up Down Scalar (UDS)

Look Up Table (LUT)

Blend ROP Unit (BRU)

Blend ROP Sub Unit (BRS)

Write Pixel Formatter (WPF)

Cubic Look Up table (CLU)

Hue Saturation value Transform (HST)

Hue Saturation value Inverse transform (HSI)

Histogram Generator -One dimension (HGO)

Histogram Generator-Two dimension (HGT)

Display Unit InterFace (LIF)

SHarPness (SHP)

User logic InterFace (UIF)

InterLeaVer (ILV)

32.5 Display Output Compare Unit (DISCOM)

R-Car H3
R-Car M3

The DISCOM calculates the CRC of input image plane and checks whether the CRC is equal to an expectation value or not.

The VSPD, which is one of video signal processing module and specified for image blending of output image, has the DISCOM. Usual use case of the DISCOM is calculation CRC of selected input plane show as following figure. DISCOM is also implemented in VSPDL.

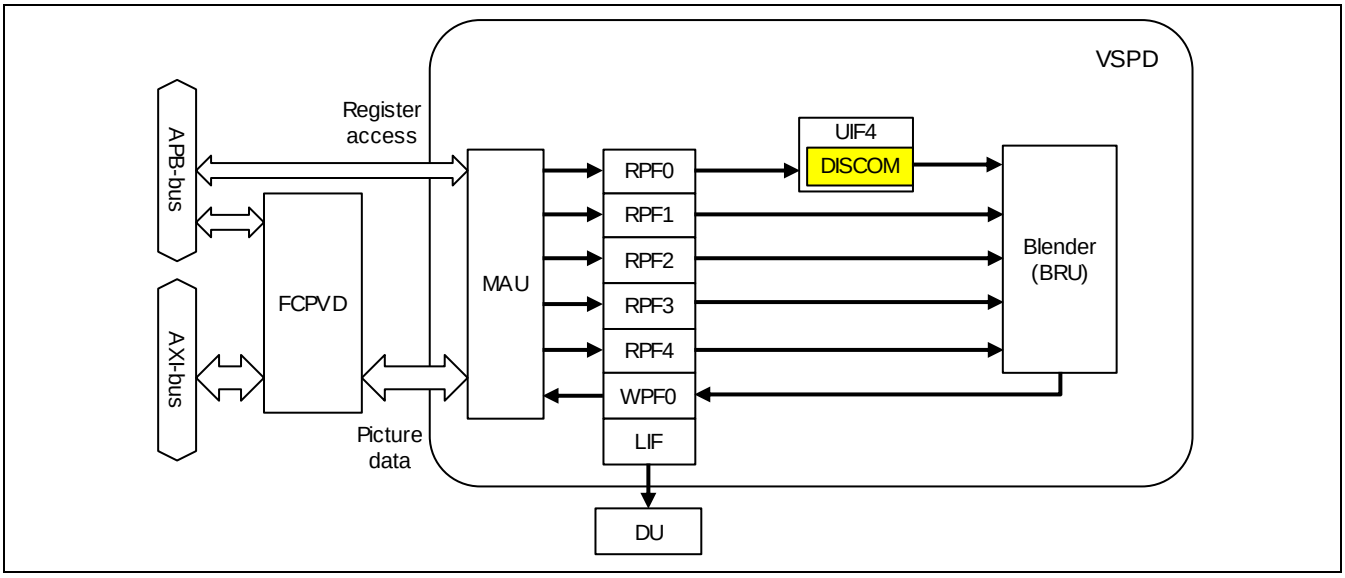


Figure 32.104 Example use case of the DISCOM

32.5.1 Features

The DISCOM has the CRC checking feature shown in following table.

Table 32.74 Main Function of the DISCOM

Item	Description
Functions	• Calculation the CRC of input image • Comparing the CRC with an expectation value • CRC calculation area is configurable.
Picture size supported	Minimum: Same as VSPD or VSPDL Maximum: Same as VSPD or VSPDL
Color format	Supported color format: • ARGB8888 • RGB888 • YCbCr444

32.5.2 Block Diagram

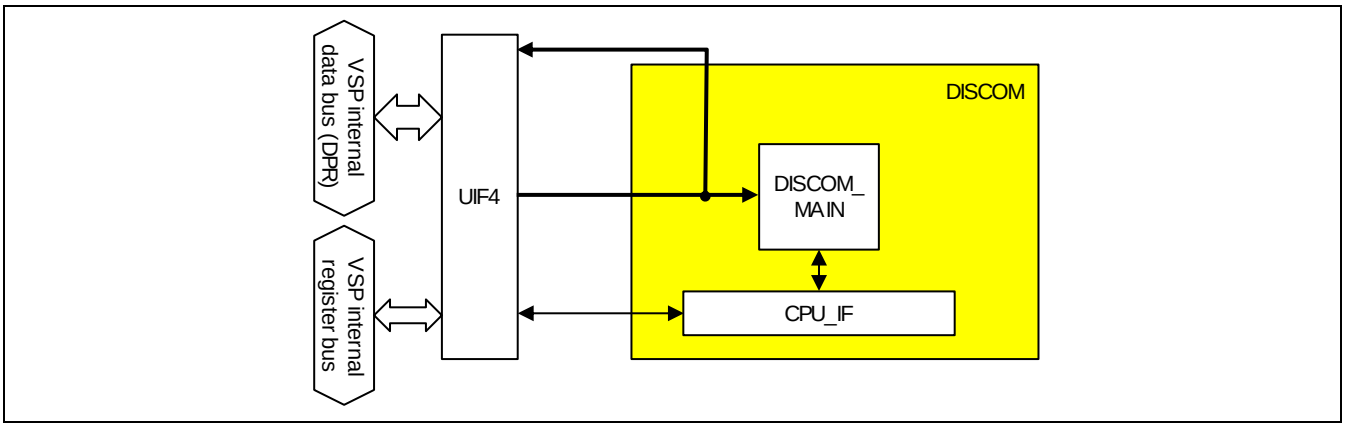


Figure 32.105 Block Diagram of DISCOM

32.5.3 Register Configuration

The DISCOM's register can be accessed via VSPD's user logic interface (UIF) register address space 4 for VSPD. The DISCOM's register can be accessed via VSPDL's user logic interface (UIF) register address space 4 and space 5 for VSPDL. All parameters should be set in the same manner as the other VSP's register, for example, setting by the display list.

Table 32.75 Register Map

Register Type	Register Name	Address Offset
DISCOM (UIF4) control	VI6_UIF4_DICOM_DOCMCR	0x1C00
	VI6_UIF4_DICOM_DOCMSTR	0x1C04
	VI6_UIF4_DICOM_DOCMCLSTR	0x1C08
	VI6_UIF4_DICOM_DOCMIENR	0x1C0C
	VI6_UIF4_DICOM_DOCMMDR	0x1C10
	VI6_UIF4_DICOM_DOCMPMR	0x1C14
	VI6_UIF4_DICOM_DOCMECRCR	0x1C18
	VI6_UIF4_DICOM_DOCMCCRCR	0x1C1C
	VI6_UIF4_DICOM_DOCMSPXR	0x1C20
	VI6_UIF4_DICOM_DOCMSPYR	0x1C24
	VI6_UIF4_DICOM_DOCMSZXR	0x1C28
	VI6_UIF4_DICOM_DOCMSZYR	0x1C2C
	VI6_UIF4_DICOM_DOCMCRCIR	0x1C30
	Setting forbidden for other UIF4 register space	0x1C00 to 0x1CFC except for above offset
DISCOM (UIF5) control	VI6_UIF5_DICOM_DOCMCR	0x1D00
	VI6_UIF5_DICOM_DOCMSTR	0x1D04
	VI6_UIF5_DICOM_DOCMCLSTR	0x1D08
	VI6_UIF5_DICOM_DOCMIENR	0x1D0C
	VI6_UIF5_DICOM_DOCMMDR	0x1D10
	VI6_UIF5_DICOM_DOCMPMR	0x1D14
	VI6_UIF5_DICOM_DOCMECRCR	0x1D18
	VI6_UIF5_DICOM_DOCMCCRCR	0x1D1C
	VI6_UIF5_DICOM_DOCMSPXR	0x1D20
	VI6_UIF5_DICOM_DOCMSPYR	0x1D24
	VI6_UIF5_DICOM_DOCMSZXR	0x1D28
	VI6_UIF5_DICOM_DOCMSZYR	0x1D2C
	VI6_UIF5_DICOM_DOCMCRCIR	0x1D30
	Setting forbidden for other UIF5 register space	0x1D00 to 0x1DFC except for above offset

32.5.4 Connected Module

Table 32.76 shows modules connected to the DISCOM.

Table 32.76 Connected Module

Module	Connected Module	Description
DISCOM (UIF4)	VSPD	VSP for image blending and output
	VSPDL	VSP for image blending and output
DISCOM (UIF5)	VSPDL	VSP for image blending and output

32.5.5 Register Description

32.5.5.1 VI6_UIFn_DICOM_DOCMCR (n = 4, 5)

[for n = 4]

R-Car H3	R-Car M3
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMCR controls the DISCOM operation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMPRU
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMPR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
16	CMPRU	0	R	This bit indicates an internal reflected bit of CMPR. The register except for DOCMCR.CMPR, DOCMCLSTR, and DOCMIENR should be updated only when CMPRU is 0. For detail, refer section 32.5.6.6 Register Update Timing.
0	CMPR	0	R/W	DISCOM execution enable. This bit is reflected to DISCOM behavior at the timing of frame staring. For detail, refer section 32.5.6.6 Register Update Timing. 0: Stop DISCOM 1: Execute DISCOM
31 to 17, 15 to1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

32.5.5.2 VI6_UIFn_DICOM_DOCMSTR (n = 4, 5)

[for n = 4]

R-Car H3	R-Car M3
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMSTR indicates the compare result of the CRC code. It is reflected at the end of frame.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP PRE	CMP ST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
1	CMPPRE	0	R	Reserved
0	CMPST	0	R	Compare result between the CRC and its expectation 0: Same as expectation 1: Not same as expectation
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

32.5.5.3 VI6_UIFn_DICOM_DOCMCLSTR (n = 4, 5)

[for n = 4]

R-Car H3	R-Car M3-W
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMCLSTR clear the DOCMSTR. When each bit of DOCMCLSTR is set to 1, the corresponding bit of DOCMSTR is cleared. Note that the clear bit takes the fixed time. Therefore after setting DOCMCLSTR, it is necessary to confirm that DOCMSTR has been cleared.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMPC LPRE	CMPC LST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
1	CMPCLPRE	0	R/W	Written value is read when reading. Keep the initial value when writing. This bit is always read as 0.
0	CMPCLST	0	R/W	Clear for CMPST status bit When this bit is set to 1, DOCMSTR.CMPST is cleared. This bit is always read as 0.
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

32.5.5.4 VI6_UIFn_DICOM_DOCMIENR (n = 4, 5)

[for n = 4]

R-Car H3	R-Car M3
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMIENR specifies the enable of the interruption.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMPP REIEN	CMP IEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
1	CMPPREIEN	0	R/W	Written value is read when reading. Keep the initial value when writing.
0	CMPIEN	0	R/W	Interruption enable for CMPI This bit specifies the interruption enable if DOCMSTR.CMPST becomes 1. 0: Disable CMPI interruption 1: Enable CMPI interruption
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

32.5.5.5 VI6_UIFn_DICOM_DOCMPMR (n = 4, 5)

[for n = 4]

R-Car H3	R-Car M3
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMPMR specifies the pixel data format.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	CMPDFF[1:0]		—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMPDFA[7:0]								CMPD AUF	—	—	—	SEL[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
18, 17	CMPDFF[1:0]	0	R/W	This parameter should be set to 0. 00: ARGB8888, RGB888, or YCbCr444 Others: Setting prohibited
15 to 8	CMPDFA[7:0]	0	R/W	This parameter specifies the default alpha value. It is used when CMPDAUF is 1.
7	CMPDAUF	0	R/W	This flag specifies the alpha value which is used for CRC calculation. 0: Use alpha value with pixel value 1: Use default alpha value (CMPDFA)
3 to 0	SEL[3:0]	0	R/W	This parameter should be set to 9.
31 to 19, 16, 6 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

32.5.5.6 VI6_UIFn_DICOM_DOCMECRCR (n = 4, 5)

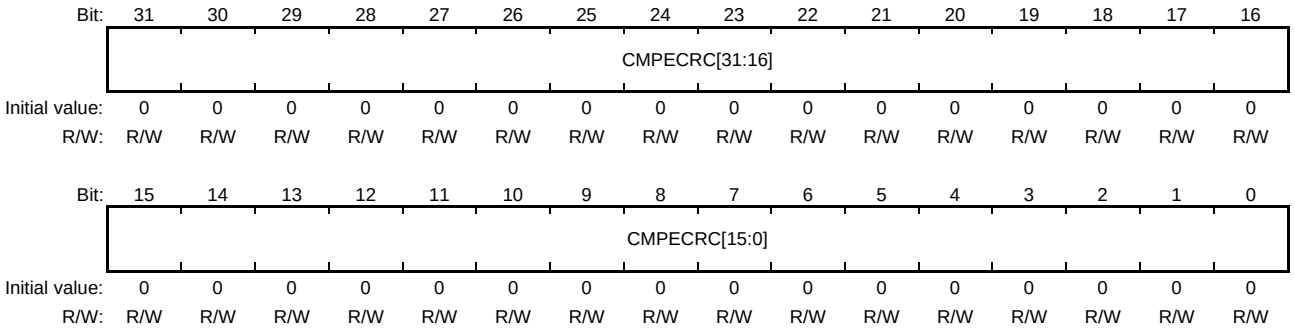
[for n = 4]

R-Car H3	R-Car M3
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMECRCR specifies the expectation value of the CRC code.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CMPECRC [31:0]	0	R/W	This parameter specifies the expectation of the CRC.

32.5.5.7 VI6_UIFn_DICOM_DOCMCCRCR (n = 4, 5)

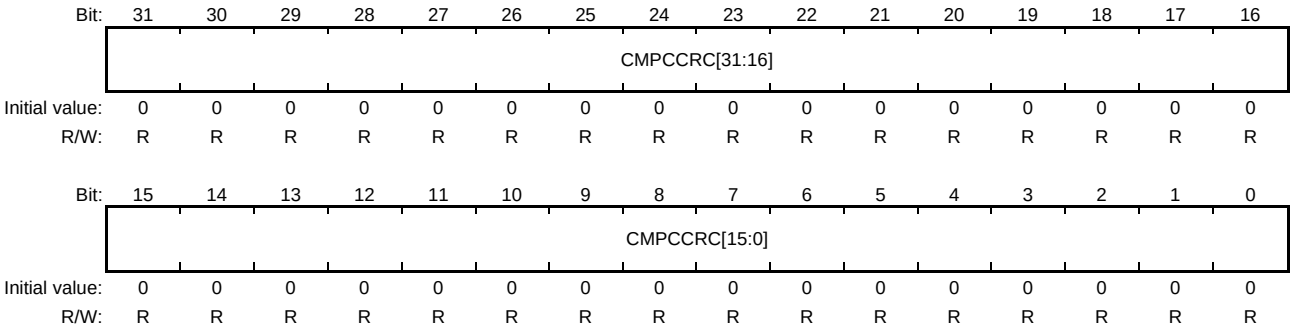
[for n = 4]

R-Car H3	R-Car M3
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMCCRCR indicates the CRC value of current image. It is reflected at the end of frame.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CMPCCRC[31:0]	0	R	This parameter indicates the CRC value of current image.

32.5.5.8 VI6_UIFn_DICOM_DOCMSPXR (n = 4, 5)

[for n = 4]

R-Car H3	R-Car M3
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMSPXR specifies horizontal offset the CRC calculation area in the image.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CMPSPX[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
12 to 0	CMPSPX [12:0]	0	R/W	This parameter specifies horizontal offset of the CRC calculation area. It should be less or equal to horizontal size of input image. Bit 12 to 11 are read only bit for R-Car M3 Horizontal offset is value of 2 * CMPSPX for R-Car M3. Horizontal offset is value of CMPSPX for other products.
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Valid bits for each product is shown below.

CMPSPX [12:0] [R-Car H3]

CMPSPX [10:0] [R-Car M3]

32.5.5.9 VI6_UIFn_DICOM_DOCMSPYR (n = 4, 5)

[for n = 4]

R-Car H3	R-Car M3
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMSPYR specifies vertical offset the CRC calculation area in the image.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CMPSPY[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
12 to 0	CMPSPY [12:0]	0	R/W	This parameter specifies vertical offset of the CRC calculation area. It should be less or equal to vertical size of input image. Bit 12 to 11 are read only bit for R-Car M3 .
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Valid bits for each product is shown below.

CMPSPY [12:0] [R-Car H3]

CMPSPY [10:0] [R-Car M3]

32.5.5.10 VI6_UIFn_DICOM_DOCMSZXR (n = 4, 5)

[for n = 4]

R-Car H3	R-Car M3
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMSZXR specifies horizontal size of the CRC calculation area.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CMPSZX[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
12 to 0	CMPSZX [12:0]	0	R/W	This parameter specifies horizontal size of the CRC calculation area. It should be less or equal to (horizontal size of input image – CMPSPX). Bit 12 to 11 are read only bit for R-Car M3. Horizontal size is value of 2 * CMPSZX for R-Car M3. Horizontal size is value of CMPSZX for other products.
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Valid bits for each product is shown below.

CMPSZX [12:0] [R-Car H3]

CMPSZX [10:0] [R-Car M3]

32.5.5.11 VI6_UIFn_DICOM_DOCMSZYR (n = 4, 5)

[for n = 4]

R-Car H3	R-Car M3
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMSZYR specifies vertical size of the CRC calculation area.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CMPSZY[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
12 to 0	CMPSZY [12:0]	0	R/W	This parameter specifies vertical size of the CRC calculation area. It should be less or equal to (vertical size of input image – CMPSPY). Bit 12 to 11 are read only bit for R-Car M3.
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Valid bits for each product is shown below.

CMPSZY [12:0] [R-Car H3]

CMPSZY [10:0] [R-Car M3]

32.5.5.12 VI6_UIFn_DICOM_DOCMMDR (n = 4, 5)

[for n = 4]

R-Car H3	R-Car M3
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMMDR specifies the compare mode of the DISCOM.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	INTHRH[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
23 to 16	INTHRH[7:0]	0	R/W	Written value is read when reading. Keep the initial value when writing.
31 to 24, 15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

32.5.5.13 VI6_UIFn_DICOM_DOCMCRCIR (n = 4, 5)

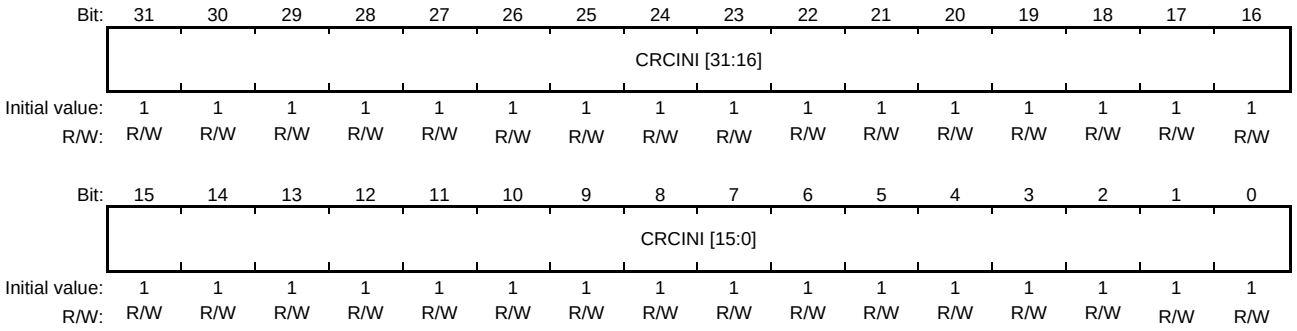
[for n = 4]

R-Car H3	R-Car M3
√	√

[for n = 5]

R-Car H3	R-Car M3
√	—

DOCMCRCIR specifies the initial value of the CRC.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CRCINI [31:0]	H'FFFF FFFF	R/W	This parameter specifies the initial value of the CRC.

32.5.6 Operation

R-Car H3
R-Car M3

32.5.6.1 Overview of process

The DISCOM calculates the CRC of arbitrary rectangular area of the input image, and compares with the expectation value.

1. If the CRC code is same as its expectation value, the display output image is as expected. This case the input image is such as graphics data, and the DISCOM is used for checking it is displayed correctly or not.

The DISCOM has the following features.

- The input image of the DISCOM can be selected from five input images of VSPD (VSPDL) by using data path routing function of the VSPD (VSPDL).
- Any CRC computation rectangular area can be specified.
- Supported color formats are ARGB8888, RGB888, and YCbCr.
- The interruption (CMPI) is occurred if the CRC value doesn't match with the expectation value.

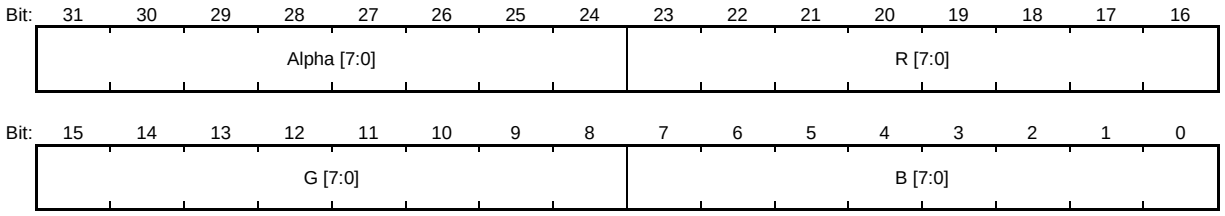
32.5.6.2 CRC Calculation

The DISCOM uses following equation to calculate the 32-bit CRC value. Each bit of the final CRC result is logically inverted.

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

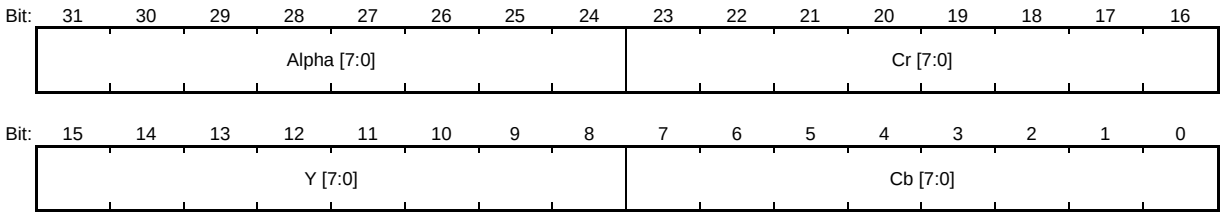
The CRC calculation is operated in pixels and the pixel order of input image is a raster scan order. The pixel data is 32-bit data and processed from LSB to MSB. The format of pixel data is shown as follows:

(a) ARGB8888/RGB888



If DOCMPMR.CMPDAUF is set to 0, the alpha value is from the data path router of the VSPD (VSPDL). Otherwise the alpha value is set as DOCMPMR.CMPDFA.

(b) YCbCr444



If DOCMPMR.CMPDAUF is set to 0, the alpha value is from the data path router of the VSPD (VSPDL). Otherwise the alpha value is set as DOCMPMR.CMPDFA.

32.5.6.3 Image Format on the External Memory

The read pixel formatter of the VSPD (VSPDL) converts the various pixel format shown in Table 32.10 and Table 32.11 to the internal pixel format of the DISCOM (shown in previous section). For the detail, refer section 32.2.6.

32.5.6.4 Setting Rectangle Region

This section describes how to set the rectangular area to the CRC calculation.

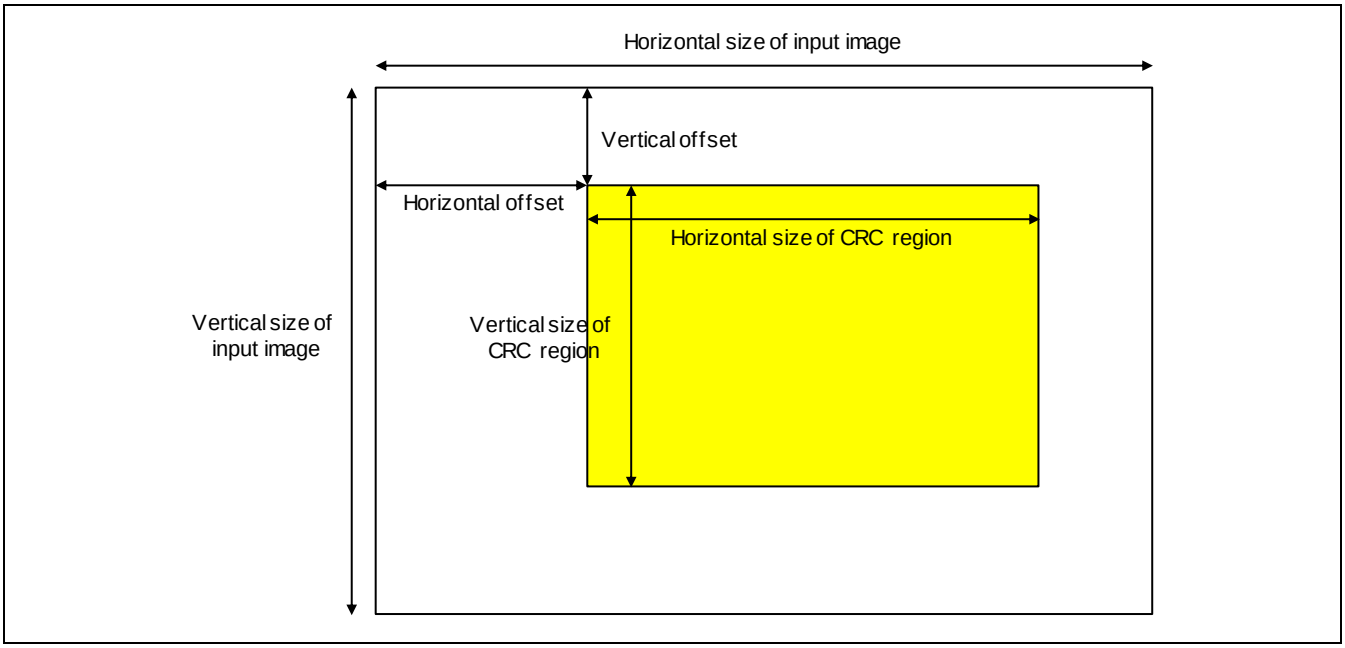


Figure 32.106 Example Case of the CRC Computation Area

Table 32.77 Register Setting for the CRC Computation Area

Word in Figure	Register of DISCOM	Description
Horizontal Size of Input Image		This parameter is horizontal size of input image for the DISCOM. It is set by VSPD's register.
Vertical size of Input Image		This parameter is vertical size of input image for the DISCOM. It is set by VSPD's register.
Horizontal Offset	DOCMSPXR	This parameter specifies horizontal offset position of the CRC calculation area from left border of the input image. The offset value is the pixel unit. Horizontal offset is value of 2 * DOCMSPXR for R-Car M3. Horizontal offset is value of DOCMSPXR is for other products.
Vertical Offset	DOCMSPYR	This parameter specifies vertical offset position of the CRC calculation area from top border of the input image. The offset value is the line unit.
Horizontal Size of CRC Region	DOCMSZXR	This parameter specifies horizontal size of the CRC calculation area. It should be less or equal to (Horizontal size of input image – Horizontal offset). The size is the pixel unit. Horizontal size is value of 2 * DOCMSZXR for R-Car M3. Horizontal size is value of DOCMSZXR for other products.
Vertical Size of CRC Region	DOCMSZYR	This parameter specifies vertical size of the CRC calculation area. It should be less or equal to (Vertical size of input image – Vertical offset). The size is the line unit.

32.5.6.5 Timing Chart of CRC Computation and Comparing

Following figure shows the timing chart example of CRC computation and comparing.

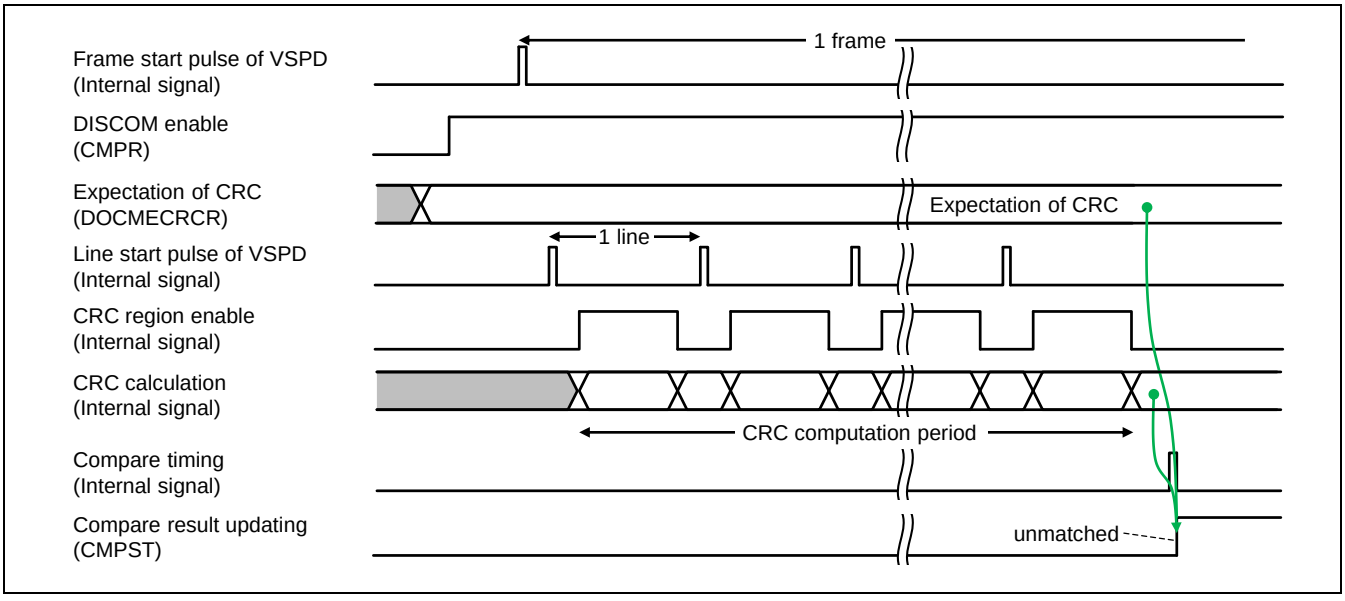


Figure 32.107 Example Timing of CRC Computation and Comparing

1. The DISCOM starts operation from the following frame after setting DOCMCR.CMPR to 1. For register update timing, refer section 32.5.6.6.
2. The CRC code is calculated in the specified rectangular area.
3. The result of the CRC code is compared with the expectation (DOCMECRCR).
4. If the CRC code doesn't match with the expectation value, DOCMSTR.CMPST bit is set to 1.

Note: When VSPD/VSPDL software reset is issued as shown in Figure 32.70, CRC calculation may be halfway finished. CRC calculation is not same with the expectation, and false error occurs as CMPST interrupt in the case. Therefore, disable VI6_UIFn_DICOM_DOCMIENR.CMPIEN before VSPD/VSPDL software reset is issued to restrain false error.

32.5.6.6 Register Update Timing

(1) Update Timing of Register Setting

All registers except for DOCMCR.CMPR are reflected in the internal register immediately. Therefore, they should be set during DOCMCR.CMPRU is 0.

The DOCMCR.CMPR is reflected in the internal register at the beginning of the frame processing. It can be updated at any time.

(2) Update Timing of Status Register

The DOCMSTR and DOCMCCRCR are updated at the end of the frame processing. The DOCMCR.CMPRU is updated at the beginning of the frame processing.

The following figure shows an example timing of register updating.

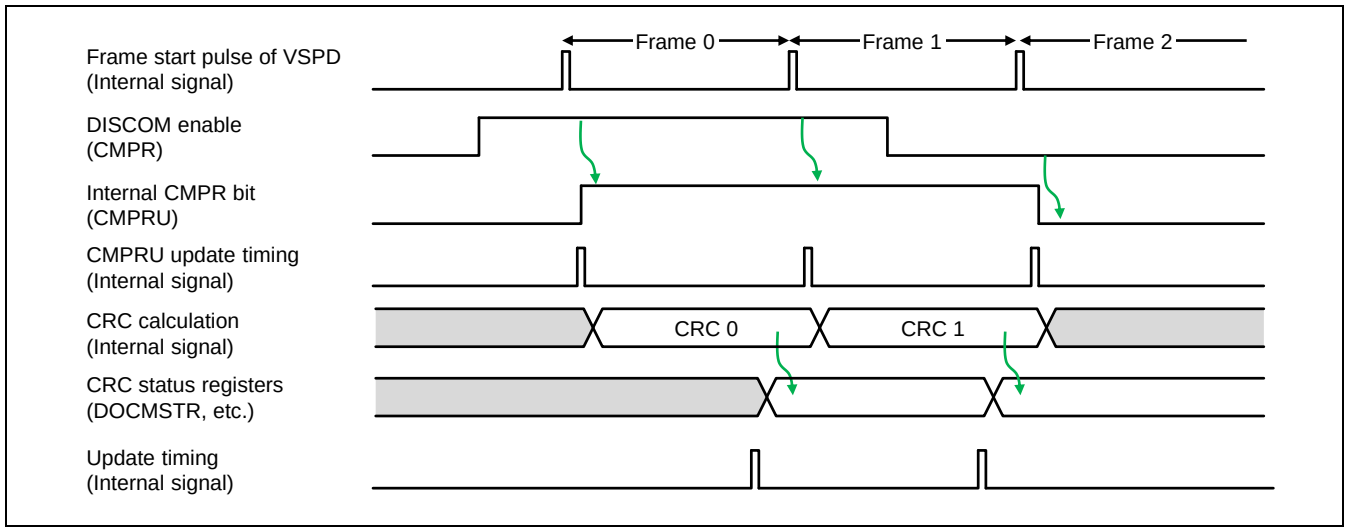


Figure 32.108 Example Timing of Register Updating

32.5.6.7 Interruption

The DISCOM has an interrupt request, CMPI. The CMPI request is occurred when both DOCMIENR.CMPIEN and DOCMSTR.CMPST are set to 1.

32.5.7 Usage Notes

32.5.7.1 Notation of register setting

Set 9 to VI6_UIFn_DICOM_DOCMPMR.SEL[3:0] (Section 32.5.5.5) before starting VSP2 in case of using UIFn (DISCOM). Otherwise, VSP may not work correctly.

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