Agenda

• Introduction
• Upstream Status
• What works
• Work in progress
• Q/A
RISC-V (risk-five)

- “Fifth” RISC ISA from Berkeley
- 32, 64 and 128 bits wide instruction sets
- little-endian by default
- Specifications
  - https://riscv.org/specifications/
- RV32I and RV64I + Extensions
  - M - Integer Mult/Div
  - A - Atomic Memory access
  - F - Floating point (single precision)
  - D - Floating point (Double precision)
  - C - Compressed
- Concatenate to represent ISA
  - E.g. RV64IMAFD
  - ‘G’ is abbreviation for ‘IMAFD’
- RV64GC is generally supported ISA by major distros e.g. (Fedora, Debian, …)
- Non-standard extensions begin with ‘X’
  - E.g. RV64GXargle_Xbargle
**Tools**

- Binutils – 2.28
- GCC – 7.0
- GLIBC – 2.27
  - Rv32i – 2.28
- Newlib – 3.0.0
- Qemu - 2.12.0
- GDB – 8.2
  - Baremetal support only
    - riscv*-*-elf
Boot Loaders

- Coreboot
  - Supports RISC-V upstream

- U-Boot – 2018.11
  - RISC-V virt board
  - Support is Upstream

- PK/BBL (Proxy Kernel/Berkeley Boot Loader)
  - [https://github.com/riscv/riscv-pk](https://github.com/riscv/riscv-pk)
RISC-V Linux Kernel Port

- Stable ABI in upstream since 4.15
- 4.19 contains drivers for Qemu “virt” board
- Major Contributors
Operating Systems - Zephyr

- [https://docs.zephyrproject.org/latest/boards/riscv32/index.html](https://docs.zephyrproject.org/latest/boards/riscv32/index.html)
  - SiFive HiFive1
  - Microsemi M2GL025 Mi-V
  - RISCV32 Emulation (QEMU)
  - Zedboard Pulpino

- **Released in 1.13.0**
- **Now Included in Standard SDK releases**
Distribution Ports – cross-distro Defaults

• Uses RV64GC - LP64 ABI
• Little-Endian
• Embedded Linux Distributions
  – Have RV32I ABI variants
  – More…
Operating Systems - Fedora

- [https://fedoraproject.org/wiki/Architectures/RISC-V](https://fedoraproject.org/wiki/Architectures/RISC-V)
- Instruction of installation:
  - [https://fedoraproject.org/wiki/Architectures/RISC-V/Installing](https://fedoraproject.org/wiki/Architectures/RISC-V/Installing)
- Info about Bootstrapping and Building
  - Bootstrap finished in March’18
  - Koji build farm is up
    - Fedora 29/Rawhide packages building using koji
      - [http://fedora-riscv.tranquility.se/koji/](http://fedora-riscv.tranquility.se/koji/)
  - Self-hosted
    - HiFive Unleashed
    - QEMU
Operating Systems - Debian

- https://wiki.debian.org/RISC-V
OpenEmbedded/Yocto

- First RISC-V Linux Distro
  - https://riscv.org/2015/01/a-linux-distribution-for-risc-v/
  - Poky Fork (yocto Project Reference Distro)
- Core Support up-streamed - 2.5 release
- BSP/Architecture Layer - (meta-riscv)
  - https://github.com/riscv/meta-riscv
  - QEMU machine
  - SiFive Freedom U540
  - Application Development Cross SDK
  - On device SDK
  - Baremetal rv32 and rv64 targets
    - Generates bare-metal SDKs useful for RTOSes e.g. zephyr
- Current Tuning
  - RV32, RV64
- Continuous Integration
  - In progress
- World Builds
  - http://errors.yoctoproject.org/Errors/Build/70151/
NOTE: Ran 16 tests in 18.662s
NOTE: FAILED
NOTE: (failures=2, skipped=2)
DEBUG: Stopping logging thread
DEBUG: Stop event received
DEBUG: Tearing down logging thread
DEBUG: Sending SIGTERM to runqemu
RESULTS:
RESULTS - connman.ConnmanTest.test_connmand_help - Testcase 961: PASSED (0.31s)
RESULTS - connman.ConnmanTest.test_connmand_running - Testcase 221: PASSED (0.30s)
RESULTS - date.DateTest.test_date - Testcase 211: PASSED (0.99s)
RESULTS - df.DfTest.test_df - Testcase 234: PASSED (0.28s)
RESULTS - gi.GObjectIntrospectionTest.test_python - Testcase -1: SKIPPED (0.00s)
RESULTS - oe_syslog.SyslogTest.test_syslog_running - Testcase 201: PASSED (0.28s)
RESULTS - oe_syslog.SyslogTestConfig.test_syslog_logger - Testcase 1149: PASSED (0.51s)
RESULTS - oe_syslog.SyslogTestConfig.test_syslog_restart - Testcase 1150: PASSED (0.41s)
RESULTS - oe_syslog.SyslogTestConfig.test_syslog_startup_config - Testcase 202: PASSED (1.56s)
RESULTS - opkg.OpkgRepoTest.test_opkg_install_from_repo - Testcase -1: PASSED (7.24s)
RESULTS - parselogs.ParseLogsTest.test_parselogs - Testcase 1059: FAILED (3.43s)
RESULTS - ping.PingTest.test_ping - Testcase 964: PASSED (0.11s)
RESULTS - ptest.PtestRunnerTest.test_ptestrunner - Testcase 1600: SKIPPED (0.25s)
RESULTS - scp.ScpTest.test_scp_file - Testcase 220: PASSED (1.44s)
RESULTS - ssh.SSHTest.test_ssh - Testcase 224: PASSED (0.70s)
RESULTS - xorg.XorgTest.test_xorg_running - Testcase 1151: FAILED (0.58s)
SUMMARY:
core-image-sato () - Ran 16 tests in 18.664s
core-image-sato - FAIL - Required tests failed (skipped=2)
ERROR: core-image-sato - FAILED - check the task log and the ssh log
DEBUG: Python function do_testimage finished
ERROR: Function failed: do_testimage

Stdout:
Machine information:
*******************************
Machine name: qemuriscv64
CPU:
Arch: riscv64
Physical cores:
Logical cores: 0
*******************************
Buildroot

- [https://github.com/riscv/riscv-buildroot](https://github.com/riscv/riscv-buildroot)
- Use ‘riscv-start’ branch
- Submitted Upstream
- RV32 port
  - Submitted
Ongoing Effort

- RISC-V LLVM
- [https://github.com/lowRISC/riscv-llvm](https://github.com/lowRISC/riscv-llvm)
  - Experimental support is up-streamed
  - Full patch-set upstreaming is going on
  - LLD port has been submitted
Ongoing Effort

- Musl C library support
- https://github.com/riscv/riscv-musl
- Upstream submission Under Review
Ongoing Effort

• OpenOCD
  – Multi-core, 64-bit

• GDB (Linux)
Ongoing Effort

- UEFI
- Grub
- V8
- Node.js
- Rust
Contributions

• Unique Contributors to Linux arch ports (4.18)
  – X86 - 1908
  – ARM - 3053
  – MIPS - 906
  – PPC - 1462
  – RISCV - 31 --> We need to get this number up
Find out more !!!

- Latest Software Status
  - https://riscv.org/software-status/
- Cores and SOCs overview
  - https://riscv.org/risc-v-cores/
- Mailing List
  - linux-riscv@lists.infradead.org
Get Involved

• Standards work (ABI, spec etc.)
• Improve/upstream Linux distribution support
• Port more software packages to RISC-V
• **Most Software is Upstream!**
  – Use a project’s regular communication mechanisms
• **Specific to RISC-V**
  – https://github.com/riscv/: Contains in-progress ports
  – sw-dev@groups.riscv.org: Software discussion
  – patches@groups.riscv.org: Patches to RISC-V ports
  – #riscv on Freenode: General RISC-V discussion
  – linux-riscv@lists.infradead.org: RISC-V Linux Port
• **Stack Overflow**
  – https://stackoverflow.com/questions/tagged/riscv
Monday, October 22 • 18:00 - 18:40

BoF: RISC-V SW Ecosystem Status and Needs - Atish Patra, Western Digital; Olof Johansson, Palmer Dabbelt & Paul Walmsley, RISC-V
Seeds of Change (Some 25+ years ago)

- [https://groups.google.com/forum/#!msg/comp.os.minix/dINtH7RRrGA/SwRavCzVE7gJ](https://groups.google.com/forum/#!msg/comp.os.minix/dINtH7RRrGA/SwRavCzVE7gJ)
- 22M+ Lines of Code
- 14K+ contributors
- Unprecedented Development Velocity
- Most Successful Open Source Software Project
History Tends to repeat 😊

Usually when forgotten
But sometimes to build upon proven ways
Thank you
Khem Raj <raj.khem@gmail.com>