GENERIC PHY FRAMEWORK

Kishon Vijay Abraham I



About Me

- I'm Kishon Vijay Abraham
 - Signed-off-by: Kishon Vijay Abraham I <kishon@ti.com>
- Working in Texas Instruments since 2007
- Contributing to linux kernel for the past four years
- Develop and Maintain PHY Subsystem (drivers/phy)
- Develop and Maintain PCIe glue for DRA7xx
- USB DWC3 driver support in u-boot
- Presented a paper on "USB Debugging and Profiling Techniques" in ELCE 2012 and "Generic PHY Framework: An Overview" in ELCE 2014



Agenda

- Introduction
- Building blocks of PHY
- PHY Integration
- Existing Mechanisms
- Introduction to Generic PHY Framework
- Using Generic PHY Framework
- Generic PHY Framework Internals
- Upcoming

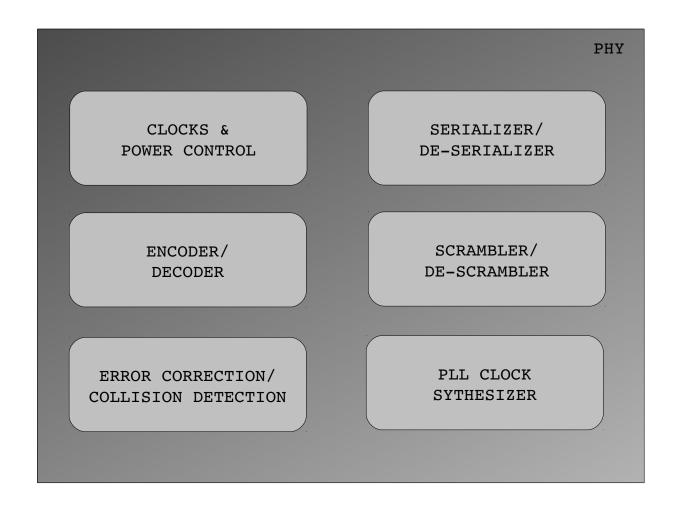


Introduction

- PHY is an abbreviation for physical layer
- Responsible for transmitting data over a physical medium
- PHY connects the device controller with the physical medium
 - USB
 - SATA
 - PCIE
 - ETHERNET



BUILDING BLOCKS



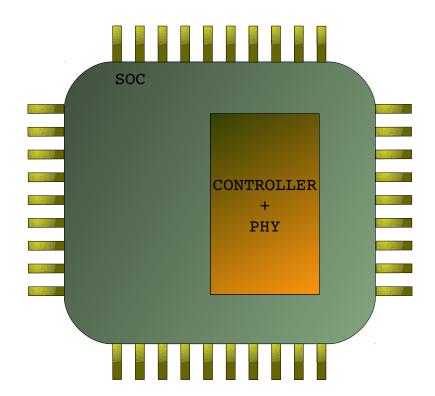
PHY INTEGRATION

- PHY integrated within the controller
- PHY integrated within the SoC
- PHY external to the SoC



PHY WITHIN THE CONTROLLER

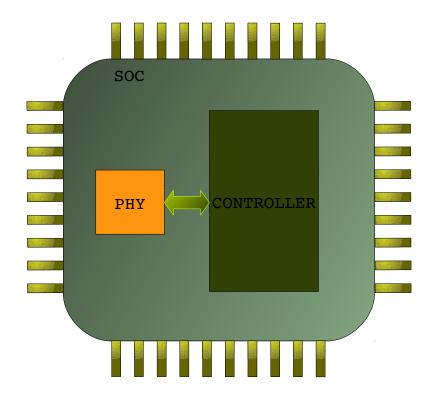
- Shares the same address space with the controller
- No separate PHY driver is required





PHY WITHIN THE SoC

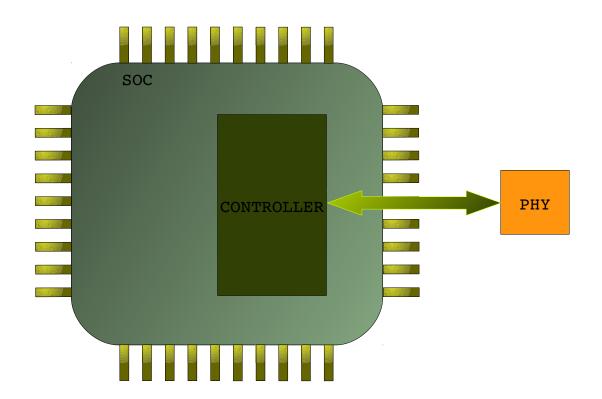
- Connected to the controller using UTMI, PIPE3 interface specification
- Should have a separate PHY driver





PHY EXTERNAL TO THE SOC

- Connected to the controller using ULPI etc..
- Should have a separate PHY driver





Existing Mechanisms

- USB: USB PHY library
 - Comprehensive library with dt and non-dt support
 - Can be used only with USB PHYs
- PHYs are programmed in the controller driver itself
 - PHY and controller are tightly bound. Changing the PHY IP will break compatibility.
- Function pointers are passed in platform data to control PHY
 - Not possible with dt

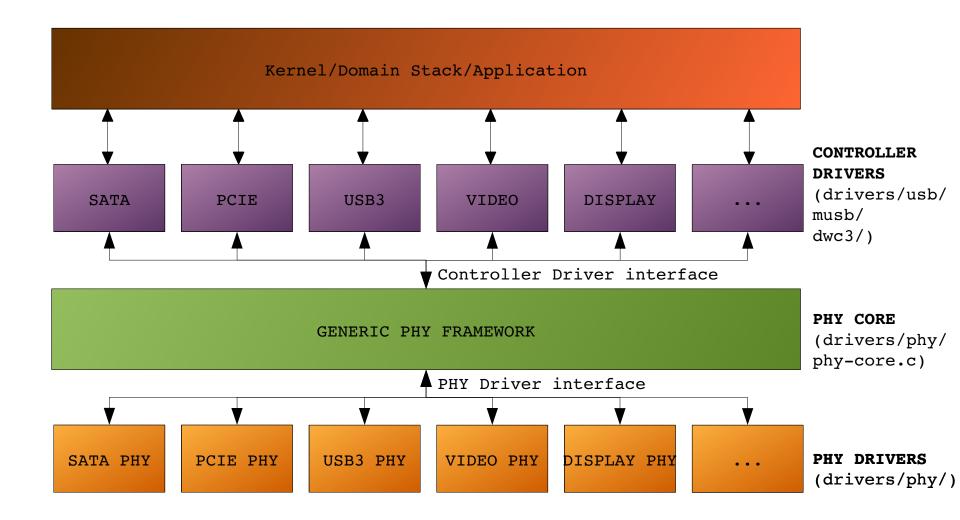


Generic PHY Framework

- PHYs integrated outside the controller
- Allows the PHY to be controlled from the controller driver
- Derived from USB PHY Framework
- Used across different subsystems USB, SATA, PCIe
- Supports dt and non-dt boot
- Invokes pm_runtime_(*) APIs



Generic PHY Framework



Using Generic PHY Framework

- Bind the controller device and PHY device
 - Device tree
 - Non device tree
- PHY drivers
 - should implement phy_ops (init, exit, power_on, power_off)
 - Register with the PHY Framework
- Controller drivers
 - Get a reference to the PHY
 - Invoke PHY framework APIs (phy_init, phy_exit, phy_power_on, phy_power_off)



Device Tree

- PHY device node
 - #phy-cells: Number of cells in the PHY specifier
- Controller device node
 - phys: list of phandles to the PHY device
 - phy-names: the names of the PHY corresponding to the phandle present in the in the phys property
- Device tree binding documentation

Documentation/devicetree/bindings/phy/phy-bindings.txt



Device Tree: Example 1

```
phy {
    compatible = "phy";
    ...
    #phy-cells = <0>;
}

controller {
    compatible = "controller";
    ...
    phys = <&phy>;
    phy-names = "phy";
}
```

Device Tree: Example 2

```
phy1 {
   compatible = "phy1";
   #phy-cells = <0>;
}
phy2 {
   compatible = "phy2";
   \#phy-cells = <1>;
}
controller {
   compatible = "controller";
   phys = <&phy1> <&phy2 PHY TYPE>;
   phy-names = "phy1", "phy2";
}
```

Device Tree: Example 3

```
phy_provider {
    compatible = "phy_provider";
    /* implement multiple PHYs: PHY_TYPE1 and PHY_TYPE2 */
    #phy-cells = <1>;
    ...
    ...
}

controller {
    compatible = "controller";
    ...
    phys = <&phy_provider PHY_TYPE1> <&phy_provider PHY_TYPE2>;
    phy-names = "phy1", "phy2";
}
```

Non Device Tree

Mapping should be created at runtime by using the following API

- Should have a reference to the PHY and the device name of the controller device.
- Used only in two places
 - dwc3 host
 - twl4030 USB PHY

Sample PHY driver

```
drivers/phy/phy-sample.c
static int sample phy init(struct phy *phy) {
    /* Initialize Sample PHY */
}
static int sample phy power on(struct phy *phy) {
    /* Enable clocks and
       power on Sample PHY */
}
static int sample phy power off(struct phy *phy) {
    /* Disable clocks and
       power off Sample PHY */
}
static int sample phy exit(struct phy *phy) {
    /* Sample PHY cleanup */
}
```

Sample PHY driver

```
struct phy ops sample phy ops {
    .init = sample phy init,
    .power on = sample phy power on,
    .power off = sample phy power off,
    .exit = sample phy exit,
};
/* Sample PHY specific implementation of of xlate.
 * sets the PHY to the mode obtained from of phandle args.
 * If the PHY provider implements multiple PHYs, then this of xlate should
 * find the correct PHY from the np present in of phandle args and return it
 */
static struct phy *sample phy xlate(struct device *dev,
                                   struct of phandle args *args) {
    sample->mode = args->args[0];
    return sample->phy;
}
```

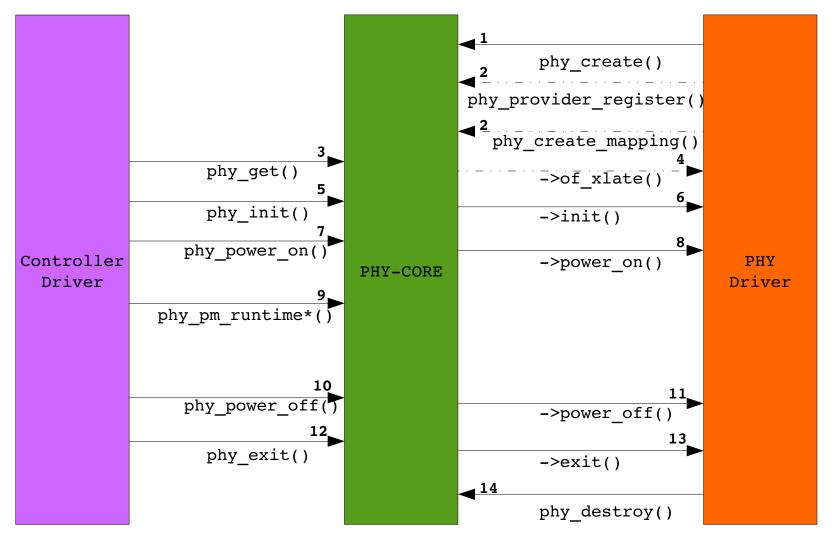
Sample PHY driver

```
static int sample phy probe(struct platform device *pdev) {
    phy = devm phy create(dev, dev->of node, &sample phy ops);
    if (dev->of node) {
        /* use default implementation of of xlate if the device tree node
         * represents a single PHY and if the PHY driver does not want to
         * receive any arguments that's added along with the phandle
         */
        // phy provider = devm of phy provider register(phy->dev,
                           of phy simple xlate);
        phy provider = devm of phy provider register(phy->dev,
                       sample phy xlate);
    } else {
        phy create lookup(phy, "phy", "sample-controller");
```

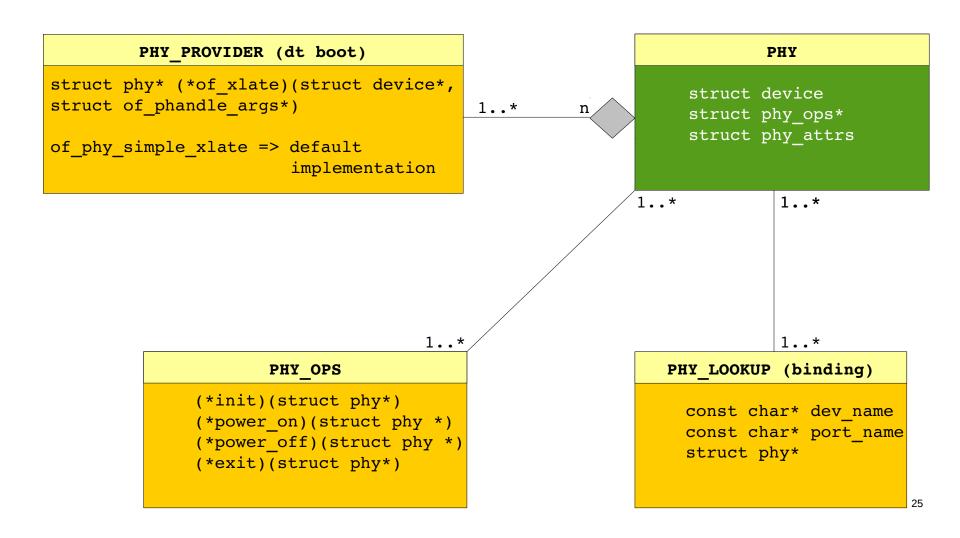
Sample Controller driver

```
drivers/<controller>/controller-sample.c
static int sample controller probe(struct platform device *pdev) {
        phy = devm phy get(dev, "sample-phy");
}
int sample controller init() {
    /* controller initialization goes here */
    phy init(phy);
}
int sample controller start transfer() {
    phy power on(phy);
    /* program the controller to start transfer */
}
int sample controller complete transfer() {
    /* free buffer etc */
    phy power off(phy);
```

Sequence Diagram

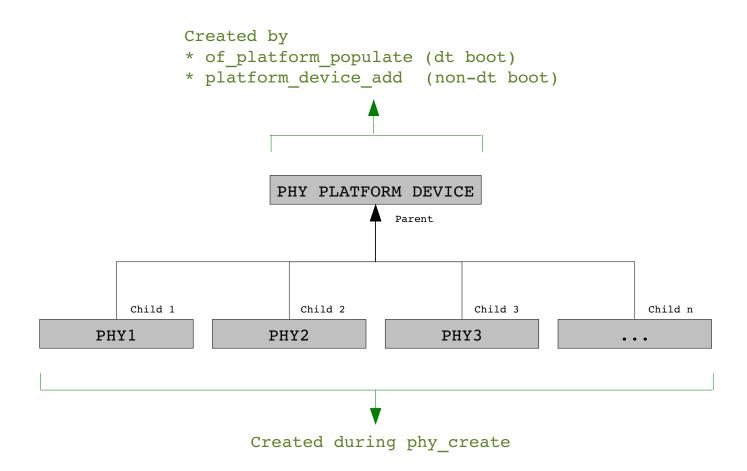


Phy-core Internals





PHY DEVICE MODEL



Upcoming

- ULPI PHY support
- Handling USB specific PHY functionality



Upstreamed PHY drivers (4.0)

РНУ	Domain	Vendor
Kona PHY	USB2	Broadcom
Berlin PHY	SATA	Marvell
Exynos PHY	USB2, SATA, DISPLAY,	Samsung
HIX5HD2 SATA PHY	SATA	Hisilicon
МІРНУ365	SATA, PCIE	STMicroelectronics
MVEBU PHY	SATA	Marvell
OMAP USB2 PHY	USB2	Texas Instruments
APQ8064 PHY	SATA	Qualcom
IPQ806X PHY	SATA	Qualcom
S5PV210 PHY	USB2	Samsung
SPEAR1310/1340 MIPHY	SATA, PCIE	STMicroelectronics
SUN4I USB PHY	USB	Allwinner
TI PIPE3	SATA, PCIE, USB3	Texas Instruments
X-GENE PHY	SATA	Applied Micro

Upstreamed PHY drivers (4.0) cont..

РНҮ	Domain	Vendor
Armada375 PHY	USB2	Marvell
KONA PHY	USB2	Broadcom
Rockchip PHY	USB2	Rockchip
RCAR PHY	USB	Renesas
QCOM UFS PHY	UFS	Qualcom

Acknowledgements

- Felipe Balbi
- Greg KH
- Linux Community



References

- drivers/phy/
- Documentation/phy.txt
- Documentation/devicetree/bindings/phy/phy-bindings.txt
- PIPE3 specification: http://www.intel.in/content/dam/www/public/us/en/documents/white-pape rs/phy-interface-pci-express-sata-usb30-architectures.pdf
- Device tree specification: https://www.power.org/documentation/epapr-version-1-1/
- Device tree for Dummies: https://www.youtube.com/watch?v=m NyYEBxfn8



THANK YOU

For Queries and Feedback

kishon@ti.com, kishonvijayabraham@gmail.com

