Common OCD pinouts:

NOTE: Macraigor Systems accepts NO responsibility for the accuracy
of the following information. These are the pinouts that our devices use, but a semiconductor manufacturer may change these specifications at any time. We strongly recommend that you use the OCD header specified by the semiconductor manufacturer and refer to this list before connecting to your target.

General Notes:

- Unless otherwise indicated, all headers are male dual-row Berg style connectors on 0.1" centers.
- We do not specify the use of pull ups or pull downs on any signals although they may be needed. Check with the chip manufacturer.
- TVcc pins should be the I/O ring voltage. This signal is used to determine the electrical characteristics of the other signals. If
  you must current limit this line, allow the probe at least 2 mA.
- Unless otherwise indicated, RESET\ or HRESET\ is an open collector signal from the probe to the target. It should directly drive the target processor and not drive power-on reset circuits
  or the like.
- If you are building your own board, place the header as close to the processor as possible, use short traces of approximately
  equal length on all clock and data signals.

Pins are identified by number and type.

- o = output from target processor to OCD interface
- i = input to target processor from OCD interface
- p = power pin
- oc = open collector driven from OCD interface, either
  floating or actively held low
- nc = not connected, ie: not driven nor read by OCD interface
- k = key, pin is typically missing from the target board

“COP” pinout for Motorola PowerPC 6xx, 7xx, 8xxx and IBM PowerPC 6xx and 7xx. IBM also refers to this connection as RISCWatch.

TDO	o	1	2	i	QACK
TDI	i	3	4	i	TRST\
HALTED	o	5	6	p	TVcc
TCK	i	7	8	nc	
TMS	i	9	10	nc	
SRESET\	i	11	12	p	GND
HRESET\	oc	13	14	nc	
CKSTP_OUT	o	15	16	p	GND

IBM 4xx (IBM also calls this RISCWatch)

TDO	o	1	2	nc	
TDI	i	3	4	i	TRST\
HALTED	o	5	6	p	TVcc
TCK	i	7	8	nc	
TMS	i	9	10	nc	
HALT	i	11	12	p	GND
SRESET\	oc	13	14	k	KEY
	nc	15	16	p	GND

“BDM” for Motorola MPC8xx, MPC5xx

NOTE: It is vital that pins 1 and 6 properly reflect the status of the target processor immediately following RESET. Some processors have configurable pins (MPC8xx, etc.) that are specified by a reset configuration word at the time of reset. These pins must be set properly and must ALWAYS reflect the status of the processor correctly. Check the ‘hardware reset configuration word’ in the Motorola User’s manual.

FRZ or VFLS0	o	1	2	o	SRESET\
GND	p	3	4	i	DSCK
GND	p	5	6	o	FRZ or VFLS1
RESET\	oc	7	8	i	DSDI
TVcc	p	9	10	o	DSDO

“OnCE” – On Chip Emulation for Motorola DSP, M•CORE

TDI	i	1	2	p	GND
TDO	o	3	4	p	GND
TCK	i	5	6	p	GND
	nc	7	8	nc	
RESET\	oc	9	10	i	TMS
TVcc	p	11	12	p	GND
	nc	13	14	i	TRST\

ARM

There are two standard ARM pinouts, an older 14 pin specification and a newer 20 pin specification.

TVcc	p	1	2	p	GND
TRST\	i	3	4	p	GND
TDI	i	5	6	p	GND
TMS	i	7	8	p	GND
TCK	i	9	10	p	GND
TDO	o	11	12	oc	RESET\
TVcc	p	13	14	p	GND

OR

TVcc	p	1	2	nc	
TRST\	i	3	4	p	GND
TDI	i	5	6	p	GND
TMS	i	7	8	p	GND
TCK	i	9	10	p	GND
	nc	11	12	p	GND
TDO	o	13	14	p	GND
RESET\	oc	15	16	p	GND
	nc	17	18	p	GND
	nc	19	20	p	GND

MIPS – EJTAG 2.5

There are many MIPS OCD headers in use. This is the one specified by MTI for EJTAG 2.5

TRST\	i	1	2	p	GND
TDI	i	3	4	p	GND
TDO	o	5	6	p	GND
TMS	i	7	8	p	GND
TCK	i	9	10	p	GND
RESET\	oc	11	12	k	key
DINT	I	13	14	p	TVcc

Toshiba's MIPS header

This header uses a pin spacing of 0.05".

TRST\	i	1	2	p	GND
TDI	i	3	4	p	GND
TDO	o	5	6	p	GND
TMS	i	7	8	p	GND
TCK	i	9	10	nc	
TVcc	p	11	12	nc	
RESET\	oc	13	14	nc	
	nc	15	16	nc	
	nc	17	18	nc	
	nc	19	20	nc	

Phillips' MIPS header

TRST\	i	1	2	p	GND
TDI	i	3	4	p	GND
TDO	o	5	6	p	GND
TMS	i	7	8	p	GND
TCK	i	9	10	p	GND
RESET\	oc	11	12	p	GND
	nc	13	14	p	GND
	nc	15	16	p	GND
	nc	17	18	p	GND
	nc	19	20	p	GND

AMD – Èlan SC520

This header uses a pin spacing of 2mm.

GND	p	1	2	p	TVcc
TCK	i	3	4	o	CMDACK
TMS	i	5	6	i	BR/TC
TDI	I	7	8	o	STOP/TX
TDO	o	9	10	o	TRIG/TRACE
SRESET\	i	11	12	k	KEY

AMD – Athlon

This header uses a pin spacing of 0.05”

TVcc	p	1	2	i	TCK
	nc	3	4	i	TMS
	nc	5	6	nc	
	nc	7	8	i	TDI
	nc	9	10	i	TRESET\
GND	p	11	12	o	TDO
DBREQ\	i	13	14	o	DBRDY
RESET\	p	15	16	i	PLLTEST\

AMD – Opteron

This header uses a pin spacing of 0.05”

GND	p	1	2	p	GND
RSVD1	o	3	4	p	GND
RSVD0	i	5	6	p	GND
DBREQ\	i	7	8	p	GND
DBRDY	o	9	10	p	GND
TCK	i	11	12	p	GND
TMS	i	13	14	p	GND
TDI	i	15	16	p	GND
TRST\	i	17	18	p	GND
TDO	o	19	20	p	GND
TVcc	p	21	22	p	GND
TVcc	p	23	24	nc	
KEY	k	25	26	nc	