MINNOW2 BOARD Rev : A1

TABLE OF CONTENTS

REVISION HISTORY:

Rev	Date	Notes
A	2014/02/13	INITIAL RELEASE LISTED ADDITIONAL COMPATIBLE PART #'s on ON SPI ROM PAGE20 UPDATED DDR3L PART # on MEM1-MEM4 on PAGES 12-13 LISTED ADDITIONAL COMPATIBLE PART #'s ON DDR3L MEMORIES MEM1-MEM4 on PAGES 12-13
A1	2014/05/02	REWORK BOARD to REV_A1 PAGE 3 - ADD U39 INVERTER FOR HPD SIGNAL PAGE 6 - ADD R354 (0 OHM RES) to tie SD3_WP with SD3_CD#, DNI J6 HEADER. PAGE 7 - CHANGE R36,R98,R99,R103 = 0 OHMS UPDATE Y1, Y2 SYMBOLS UPDATE D5, D10 SYMBOLS PAGE 8 - CHANGE I2C5/I2C6 BUS NAMES PAGE 11 - TURN AROUND and DNI J2 HEADER, CHANGE MP1 HEATSINK PAGE 12 - UPDATE 0.047uF CAP SYMBOLS and MEM2/MEM3 SYMBOLS PAGE 13 - UPDATE 0.047uF CAP, 36R0 RES and MEM1/MEM4 SYMBOLS PAGE 14 - CHANGE R182 to 100K and PU to +V1P8S and change R180/R174/R173/R157/R156/R155 to 100K PAGE 15 - DNI R166, CHANGE R28-R30 = 10K PAGE 16 - DNI R115, UPDATE U32, L1/L2 SYMBOLS PAGE 17 - ADD PCIE TEST POINT VIAS (TP19-TP24), ADD +VSB to R18, +V1P8S TO R20, STUFF R21, CHANGE R6 PU FROM +V1P8A to +V1P8S, CHANGE R7 FROM 20K to 1K, CHANGE I2C6_SCL/SDA net names PAGE 18 - UPDATE Y3, J8 SYMBOL, ADD TP17-TP18 TEST POINTS PAGE 20 - UPDATE U3, D8 SYMBOLS, CHANGE R147 to 100K and PU TO +3VSB, UPDATE I2C5_SCL/SDA NET NAMES PAGE 21 - CHANGE BOARD MTG HOLE SYMBOLS to SUPPORT 6-32 screw. PAGE 22 - DNI R289, CHANGE R308 to 33 OHMS PAGE 23 - UPDATE CAP SYMBOLS (C36,C39,C61,C62) PS PH1 OPTIMIZE 1.) CHANGE C76,C77,C87 to LOWER ESR CAP 2.) CHANGE C40,C59 FROM 0.022uF to 0.047uF 3.) CHANGE R93 FROM 3.32KOHM to 2.6KOHM 4.) CHANGE R194 FROM 33KOHM to 80.6KOHM 5.) CHANGE R247 FROM 30KOHM to 80.6KOHM 6.) CHANGE R200 FROM 3.6KOHM to 3.32KOHM PAGE 25 - CHANGE C129 TO LOWER ESR CAP PAGE 27 - UPDATE GPIO SETTINGS DOCUMENTATION

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MINNOWBOARD2

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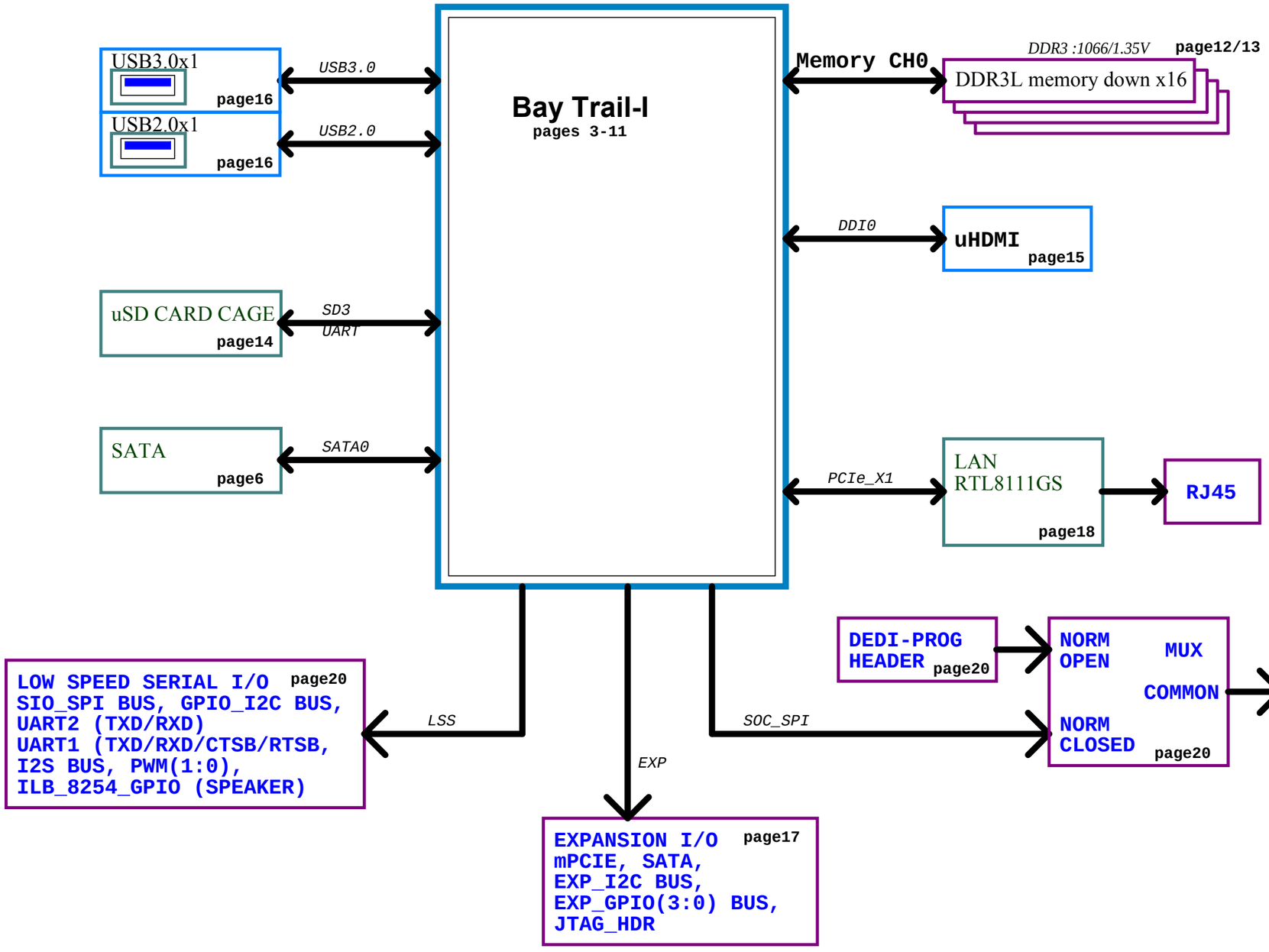

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FOR HDMI VIDEO/AUDIO,
REVERSE BIT CONNECTIONS
FROM (0:2) TO (2:0), BIT3
IS THE CLOCK SIGNAL.

STRAIGHT BIT ORDER is
for EDP ONLY
HDMI

REWORK -
ADD LVC1G14
BUFFER TO HPD
SIGNAL BEFORE
GOING TO SOC

+V1P8S
GND C375 0.1uF
U39 SN74LVC1G14DBVR
15 HDMI_HPD
GND

15 HDMI_TX2_DP
15 HDMI_TX2_DN
15 HDMI_TX1_DP
15 HDMI_TX1_DN
15 HDMI_TX0_DP
15 HDMI_TX0_DN
15 HDMI_CLK_DP
15 HDMI_CLK_DN
15 HDMI_DDCDAT
15 HDMI_DDCCLK

R217 1 2 402R DDI_RCOMP_P DDI_RCOMP_N

GND R42 1 2 0R0 GND R41 1 2 0R0
Bay Trail-I Different

GND R102 10K0 GPIO_NC13
TP15

CPU1C

AV3	(+V1P0S)	HDMI_TX2_DP	DDI0_TXP_0
AV2	(+V1P0S)	HDMI_TX2_DN	DDI0_TXN_0
AT2	(+V1P0S)	HDMI_TX1_DP	DDI0_TXP_1
AT3	(+V1P0S)	HDMI_TX1_DN	DDI0_TXN_1
AR3	(+V1P0S)	HDMI_TX0_DP	DDI0_TXP_2
AR1	(+V1P0S)	HDMI_TX0_DN	DDI0_TXN_2
AP3	(+V1P0S)		DDI0_TXP_3
AP2	(+V1P0S)		DDI0_TXN_3
AL3	(+V1P0S)		DDI0_AUXP
AL1	(+V1P0S)		DDI0_AUXN
D27	(+V1P8S)	HDMI_HPD_B	DDI0_HPD
C26	(+V1P8S)	HDMI_DDCDAT	DDI0_DDCDATA
C28	(+V1P8S)	HDMI_DDCCLK	DDI0_DDCCLK
B28	(+V1P8S)		DDI0_VDDEN
C27	(+V1P8S)		DDI0_BKLTEN
B26	(+V1P8S)		DDI0_BKLTCTL
AK13	(+V1P0S)	DDI_RCOMP_P	DDI0_RCOMP
AK12	(+V1P0S)	DDI_RCOMP_N	DDI0_RCOMP_P
AM14			RESERVED_AM14
AM13			RESERVED_AM13
AM3			RESERVED_VSS0
AM2			RESERVED_VSS1
T2			RESERVED_T2
T3			RESERVED_T3
AB3			RESERVED_AB3
AB2			RESERVED_AB2
Y3			RESERVED_Y3
Y2			RESERVED_Y2
W3			RESERVED_W3
W1			RESERVED_W1
V2			RESERVED_V2
V3			RESERVED_V3
R3			RESERVED_R3
R1			RESERVED_R1
AD6			RESERVED_AD6
AD4			RESERVED_AD4
AB9			RESERVED_AB9
AB7			RESERVED_AB7
Y4			RESERVED_Y4
Y6			RESERVED_Y6
V4			RESERVED_V4
V6			RESERVED_V6
A29		GPIO_NC13	RESERVED_A29
C29			RESERVED_C29
AB14			RESERVED_AB14
B30			GPIO_S0_NC12
C30			RESERVED_C30

BAYTRAIL_I
REV = 1.0
DISPLAY SECTION

INTEL ATOM 3825 PROCESSOR

Bay Trail-M Remove eDP Port

DDI1_TXP_0	AG3	(+V1P0S)	
DDI1_TXN_0	AG1	(+V1P0S)	
DDI1_TXP_1	AF3	(+V1P0S)	
DDI1_TXN_1	AF2	(+V1P0S)	
DDI1_TXP_2	AD3	(+V1P0S)	
DDI1_TXN_2	AD2	(+V1P0S)	
DDI1_TXP_3	AC3	(+V1P0S)	
DDI1_TXN_3	AC1	(+V1P0S)	
DDI1_AUXP	AK3	(+V1P0S)	
DDI1_AUXN	AK2	(+V1P0S)	
DDI1_HPD	K30	(+V1P8S)	GND
DDI1_DDCDATA	P30	(+V1P8S)	DDI1_DDCDAT 1 R257 2 2K20 GND
DDI1_DDCCLK	G30	(+V1P8S)	GND
DDI1_VDDEN	N30	(+V1P8S)	
DDI1_BKLTEN	J30	(+V1P8S)	
DDI1_BKLTCTL	M30	(+V1P8S)	
RESERVED_AH14	AH14		
RESERVED_AH13	AH13		
RESERVED_AF14	AF14		
RESERVED_AF13	AF13		
RESERVED_VSS2	AH3		R46 1 2 0R0 GND
RESERVED_VSS3	AH2		R43 1 2 0R0 GND
VGA_RED	BA3	(VVGA_GPIO)	
VGA_BLUE	AY2	(VVGA_GPIO)	
VGA_GREEN	BA1	(VVGA_GPIO)	
VGA_IREF	AW1		R40 357R GND
VGA_IRTN	AY3		GND
VGA_HSYNC	BD2	(VVGA_GPIO)	
VGA_VSYNC	BF2	(VVGA_GPIO)	CRT_CLK 1 R39 2 150R GND
VGA_DDCCLK	BC1	(VVGA_GPIO)	
VGA_DDCDATA	BC2	(VVGA_GPIO)	CRT_DAT 1 R38 2 150R

THIS NEEDS TO BE
357 OHMS

RESERVED_T7	T7	(V1P24S)	
RESERVED_T9	T9	(V1P24S)	
RESERVED_AB13	AB13	(V1P24S)	
RESERVED_AB12	AB12	(V1P24S)	
RESERVED_Y12	Y12	(V1P24S)	
RESERVED_Y13	Y13	(V1P24S)	
RESERVED_V10	V10	(V1P24S)	
RESERVED_V9	V9	(V1P24S)	
RESERVED_T12	T12	(V1P24S)	
RESERVED_T10	T10	(V1P24S)	
RESERVED_V14	V14	(V1P24S)	
RESERVED_V13	V13	(V1P24S)	
RESERVED_T14	T14	(V1P24S)	
RESERVED_T13	T13	(V1P24S)	
RESERVED_T6	T6	(V1P24S)	
RESERVED_T4	T4	(V1P24S)	
RESERVED_P14	P14	(V1P24S)	MCSI_RCOMP 1 R213 2 150R GND
RESERVED_K34	K34	(V1P24S)	
RESERVED_D32	D32	(V1P24S)	
RESERVED_N32	N32	(V1P24S)	
RESERVED_J34	J34	(V1P24S)	
RESERVED_K28	K28	(V1P24S)	
RESERVED_F28	F28	(V1P24S)	
RESERVED_F32	F32	(V1P24S)	
RESERVED_D34	D34	(V1P24S)	
RESERVED_J28	J28	(V1P24S)	
RESERVED_D28	D28	(V1P24S)	
RESERVED_M32	M32	(V1P24S)	
RESERVED_F34	F34	(V1P24S)	

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Bay Trail-I MCSI Port

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MINNOWBOARD2 - CPU-DDI/VGA

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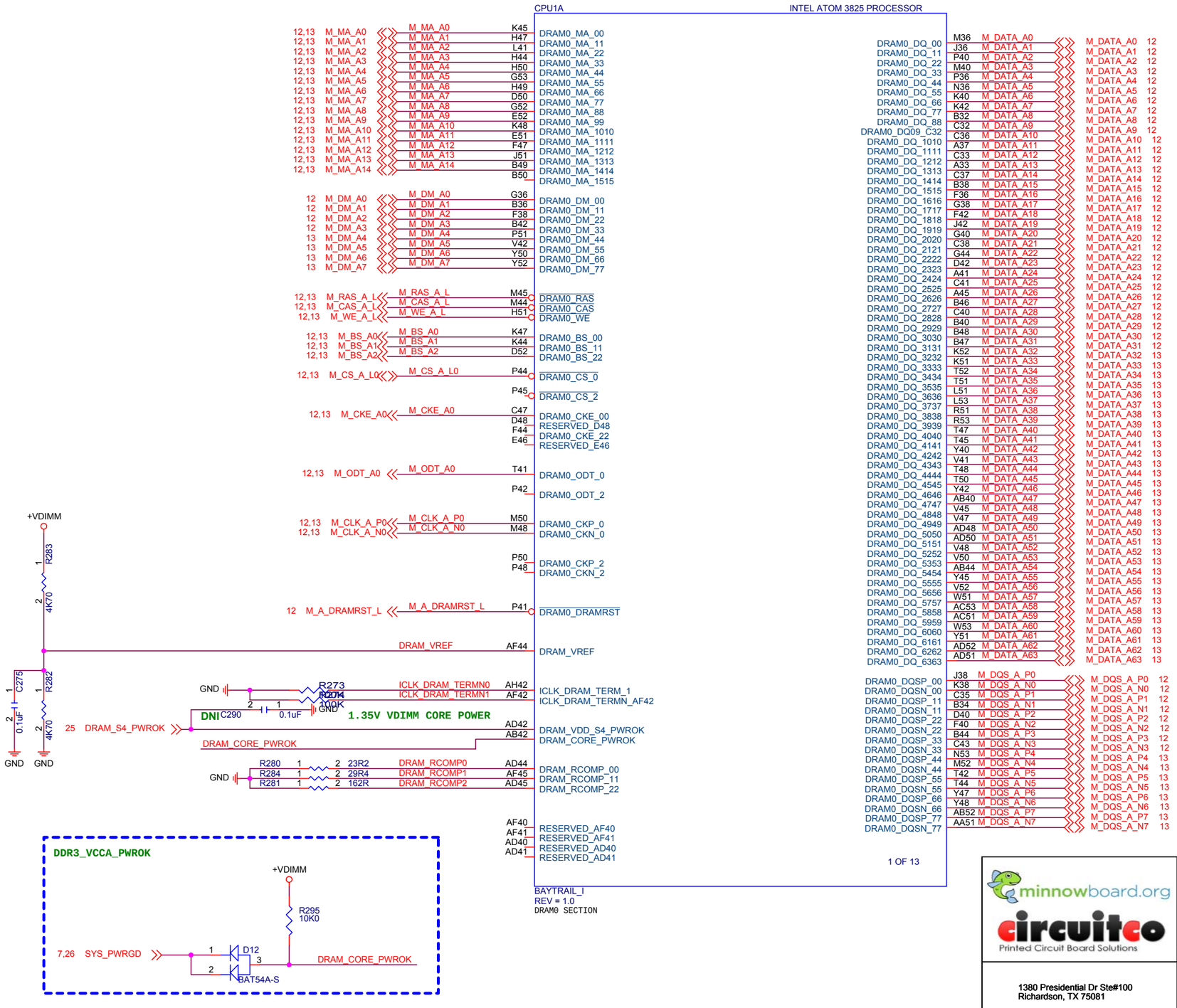

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MINNOWBOARD2 - CPU-DDR3-CHA

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CPU1B — INTEL ATOM 3825 PROCESSOR

AY45	DRAM1_MA_00	DRAM1_DQ_00	BG38
BB47	DRAM1_MA_11	DRAM1_DQ_11	BC40
AW41	DRAM1_MA_22	DRAM1_DQ_22	BA42
BB44	DRAM1_MA_33	DRAM1_DQ_33	BD42
BB50	DRAM1_MA_44	DRAM1_DQ_44	BC38
BC53	DRAM1_MA_55	DRAM1_DQ_55	BD36
BB49	DRAM1_MA_66	DRAM1_DQ_66	BF42
BF50	DRAM1_MA_77	DRAM1_DQ_77	BC44
BC52	DRAM1_MA_88	DRAM1_DQ_88	BH32
BE52	DRAM1_MA_99	DRAM1_DQ_99	BG32
AY48	DRAM1_MA_1010	DRAM1_DQ_1010	BG36
BE51	DRAM1_MA_1111	DRAM1_DQ_1111	BJ37
BD47	DRAM1_MA_1212	DRAM1_DQ_1212	BG33
BA51	DRAM1_MA_1313	DRAM1_DQ_1313	BJ33
BH49	DRAM1_MA_1414	DRAM1_DQ_1414	BG37
BH50	DRAM1_MA_1515	DRAM1_DQ_1515	BH38
		DRAM1_DQ_1616	AU36
BD38		DRAM1_DQ_1717	AT36
BH36	DRAM1_DM_00	DRAM1_DQ_1818	AV40
BC36	DRAM1_DM_11	DRAM1_DQ_1919	AT40
BH42	DRAM1_DM_22	DRAM1_DQ_2020	BA36
AT51	DRAM1_DM_33	DRAM1_DQ_2121	AV36
AM42	DRAM1_DM_44	DRAM1_DQ_2222	AY42
AK50	DRAM1_DM_55	DRAM1_DQ_2323	AY40
AK52	DRAM1_DM_66	DRAM1_DQ_2424	BJ41
	DRAM1_DM_77	DRAM1_DQ_2525	BG41
AV45		DRAM1_DQ_2626	BJ45
AV44	DRAM1_RAS	DRAM1_DQ_2727	BH46
BB51	DRAM1_CAS	DRAM1_DQ_2828	BG40
	DRAM1_WE	DRAM1_DQ_2929	BH40
AY47		DRAM1_DQ_3030	BH48
AY44	DRAM1_BS_00	DRAM1_DQ_3131	BH47
BF52	DRAM1_BS_11	DRAM1_DQ_3232	AY52
	DRAM1_BS_22	DRAM1_DQ_3333	AY51
AT44		DRAM1_DQ_3434	AP52
	DRAM1_CS_0	DRAM1_DQ_3535	AP51
AT45		DRAM1_DQ_3636	AW51
	DRAM1_CS_2	DRAM1_DQ_3737	AW53
		DRAM1_DQ_3838	AR51
BG47		DRAM1_DQ_3939	AR53
BE46	DRAM1_CKE_00	DRAM1_DQ_4040	AP47
BD44	RESERVED_BE46	DRAM1_DQ_4141	AP45
BF48	DRAM1_CKE_22	DRAM1_DQ_4242	AK40
	RESERVED_BF48	DRAM1_DQ_4343	AM41
AP41		DRAM1_DQ_4444	AP48
	DRAM1_ODT_0	DRAM1_DQ_4545	AP50
AT42		DRAM1_DQ_4646	AK42
	DRAM1_ODT_2	DRAM1_DQ_4747	AH40
		DRAM1_DQ_4848	AM45
AV50		DRAM1_DQ_4949	AM47
AV48	DRAM1_CKP_0	DRAM1_DQ_5050	AF48
	DRAM1_CKN_0	DRAM1_DQ_5151	AF50
		DRAM1_DQ_5252	AM48
AT50		DRAM1_DQ_5353	AM50
AT48	DRAM1_CKP_2	DRAM1_DQ_5454	AH44
	DRAM1_CKN_2	DRAM1_DQ_5555	AK45
		DRAM1_DQ_5656	AM52
		DRAM1_DQ_5757	AL51
AT41		DRAM1_DQ_5858	AG53
	DRAM1_DRAMRST	DRAM1_DQ_5959	AG51
		DRAM1_DQ_6060	AL53
		DRAM1_DQ_6161	AK51
		DRAM1_DQ_6262	AF52
		DRAM1_DQ_6363	AF51
		DRAM1_DQSP_00	BF40
		DRAM1_DQSN_00	BD40
		DRAM1_DQSP_11	BG35
		DRAM1_DQSN_11	BH34
		DRAM1_DQSP_22	BA38
		DRAM1_DQSN_22	AY38
		DRAM1_DQSP_33	BH44
		DRAM1_DQSN_33	BG43
		DRAM1_DQSP_44	AU53
		DRAM1_DQSN_44	AV52
		DRAM1_DQSP_55	AP42
		DRAM1_DQSN_55	AP44
		DRAM1_DQSP_66	AK47
		DRAM1_DQSN_66	AK48
		DRAM1_DQSP_77	AH52
		DRAM1_DQSN_77	AJ51

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DRAM1 SECTION

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MINNOWBOARD2 - CPU-DDR3-CHB

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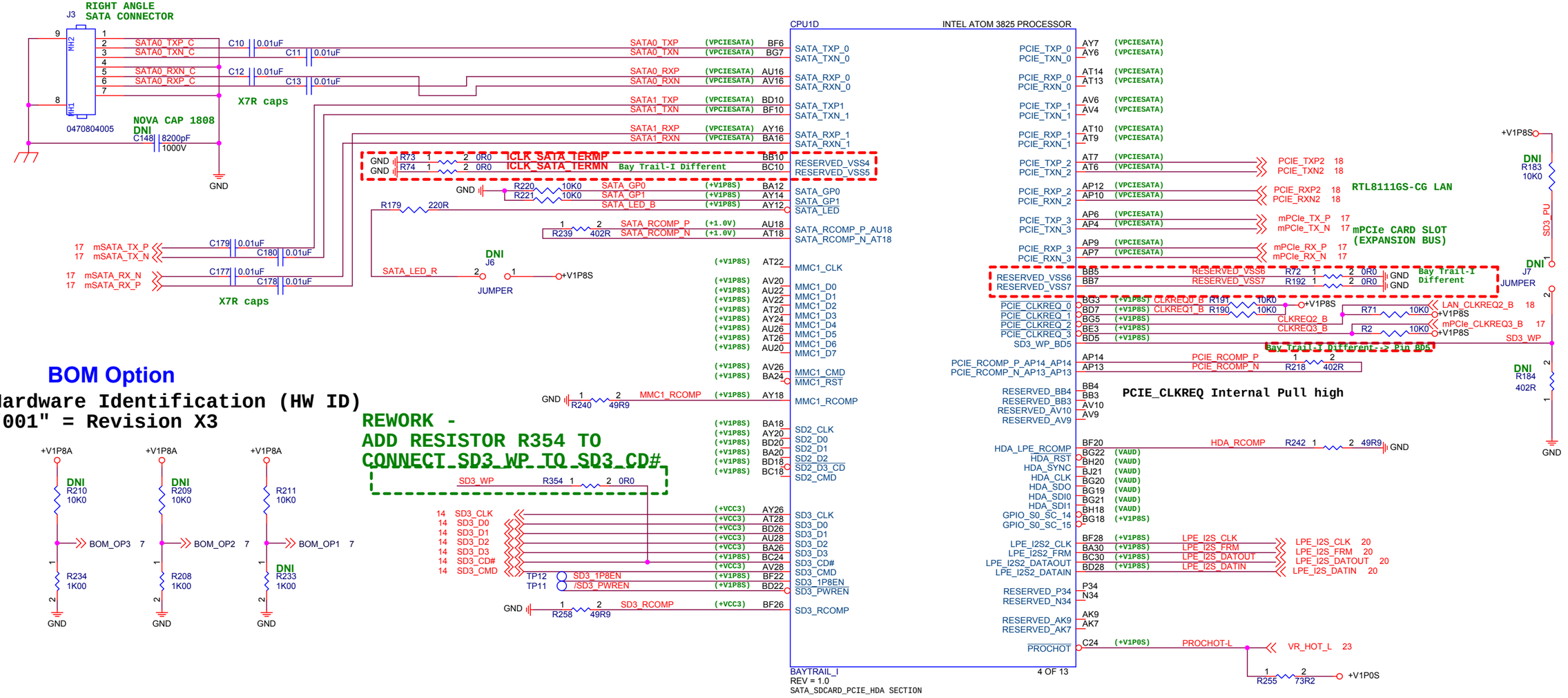
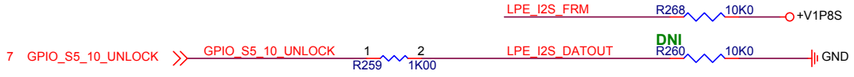


BOM Option

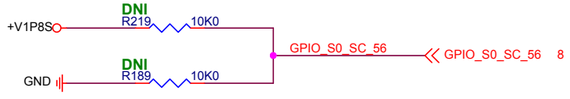
Hardware Identification (HW ID)
"001" = Revision X3

REWORK -
ADD RESISTOR R354 TO CONNECT SD3_WP TO SD3_CD#



HW STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC



Strap Pin	Function
GPIO_S0_SC63 (LPE_I2S_FRM)	BIOS Boot Selection 0=LPC *1=SPI
GPIO_S0_SC65 (LPE_I2S_DATOUT)	Security Flash Descriptors 0=Override *1=Normal Operation

Top Swap(A16 Override)

H	Top address bit is unchanged
L	Top address bit is inverted

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MINNOWBOARD2 - CPU-PE/HDA/SD/eMMC/Strap

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UPDATE
Y2 SYMBOL

Y2 25.00MHz R188 1M00 C175 27pF C176 27pF GND

XTAL25_IN AH12 ICLK_OSCIN
XTAL25_OUT AH10 ICLK_OSCOUT
AD9 RESERVED_AD9
R215 4K02 ICLK_ICOMP AD14 ICLK_ICOMP
R214 47R5 ICLK_RCOMP AD13 ICLK_RCOMP
AD10 RESERVED_AD10
AD12 RESERVED_AD12
(+V1P0S) AF6 PCIE_CLKN_00
(+V1P0S) AF4 PCIE_CLKP_00
(+V1P0S) AF9 PCIE_CLKN_11
(+V1P0S) AF7 PCIE_CLKP_11

RTL8111GS-CG LAN
18 PCIE_CLK-N2
18 PCIE_CLK-P2
(+V1P0S) AK4 PCIE_CLKN_22
(+V1P0S) AK6 PCIE_CLKP_22

EXPANSION BUS
mPCIE_CARD_SLOT
17 mPCIe_REFCLK_N
17 mPCIe_REFCLK_P
(+V1P0S) AM4 PCIE_CLKN_33
(+V1P0S) AM6 PCIE_CLKP_33
AM10 RESERVED_AM10
AM9 RESERVED_AM9

17 XDP_H_TCK R8 51R0
17 XDP_H_TRSTB R19 51R0
17 XDP_H_TMS R9 51R0
17 XDP_H_TDI R10 51R0
+V1P8A

(+V1P8S) BH7 PMC_PLT_CLK_00
(+V1P8S) BH5 PMC_PLT_CLK_11
(+V1P8S) BH4 PMC_PLT_CLK_22
(+V1P8S) BH8 PMC_PLT_CLK_33
(+V1P8S) BH6 PMC_PLT_CLK_44
(+V1P8S) BJ9 PMC_PLT_CLK_55
RTCRST_L (+RTCVCC) C12 ILB_RTC_RST
(+V1P8A) D14 TAP_TCK
(+V1P8A) G12 TAP_TRST
(+V1P8A) F14 TAP_TMS
(+V1P8A) F12 TAP_TDI
(+V1P8A) G16 TAP_TDO
(+V1P8A) D18 TAP_PRDY
(+V1P8A) F16 TAP_PREQ
AT34 RESERVED

REWORK
CHANGE
FROM 22 OHMS
to 0 OHMS

17 XDP_H_TDO
17 XDP_H_PRDYB
17 XDP_H_PREQB

To DEDIPROG HDR
AND MUX - PG20
20 SOC_SPI_CS0B-R
20 SOC_SPI_MISO-R
20 SOC_SPI_MOSI-R
20 SOC_SPI_CLK-R

DNI R99 0R0 SOC_SPI_CS0B (+V1P8A) C23 PCU_SPI_CS_00
DNI R235 0R0 SOC_SPI_CS1B (+V1P8A) C21 PCU_SPI_CS_11
R36 0R0 SOC_SPI_MISO (+V1P8A) B22 PCU_SPI_MISO
R103 0R0 SOC_SPI_MOSI (+V1P8A) A21 PCU_SPI_MOSI
R98 0R0 SOC_SPI_CLK (+V1P8A) C22 PCU_SPI_CLK
10pF C69 DNI GND

20 SOC_GPIO_S5_0 (+V1P8A) B18 GPIO_S5_0
20 SOC_GPIO_S5_1 (+V1P8A) B16 GPIO_S5_1
20 SOC_GPIO_S5_2 (+V1P8A) C18 GPIO_S5_2
(+V1P8A) A17 GPIO_S5_3
(+V1P8A) C17 GPIO_S5_4
6 BOM_OP1 (+V1P8A) C16 GPIO_S5_5
6 BOM_OP2 (+V1P8A) B14 GPIO_S5_6
6 BOM_OP3 (+V1P8A) C15 GPIO_S5_7

17 mPCIE_WAKEB
Internal Pull UP
+V1P8A DNI R1 2K20

16 SOC_USB_HOST_EN0 (+V1P8A) C13 GPIO_S5_8
16 SOC_USB_HOST_EN1 (+V1P8A) A13 GPIO_S5_9
(+V1P8A) C19 GPIO_S5_10
6 GPIO_S5_10_UNLOCK GPIO_S5_10_UNLOCK

GND 49R9 R238 GPIO_RCOMP (+V1P8S) N26 GPIO_RCOMP

CPU1E
INTEL ATOM 3825 PROCESSOR
BAYTRAIL_I
REV = 1.0
SIO_PMC_PCU_GPIO SECTION
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SoC Internal Pull high

SIO_UART1_RXD AU34 (+V1P8S) SIO_UART1_RXD 20
SIO_UART1_TXD AV34 (+V1P8S) SIO_UART1_TXD 20
SIO_UART1_RTS BA34 (+V1P8S) SIO_UART1_RTSB 20
SIO_UART1_CTS AY34 (+V1P8S) SIO_UART1_CTSB 20

SIO_UART2_RXD BF34 (+V1P8S) SIO_UART2_RXD 20
SIO_UART2_TXD BD34 (+V1P8S) SIO_UART2_TXD 20
SIO_UART2_RTS BD32 (+V1P8S)
SIO_UART2_CTS BF32 (+V1P8S)

PMC_SUSPWRDNACK D26 (+V1P8A) SUSPWRDNACK TP14 R254 10K0 VCC_UNCORE_G3_V1P8
PMC_SUSCLK0_G24 G24 (+V1P8A) PMC_SUSCLK0
PMC_SLP_S0IX F18 PMC_SLP_S0IX TP10
PMC_SLP_S4 F22 (+V1P8A) PMC_SLP_S4_L
PMC_SLP_S3 D22 (+V1P8A) PMC_SLP_S3_L
GPIO_S5_14 J20 (+V1P8A) GPIO_S514_J20 Bay Trail-I Different R237 10K0 +V1P8A
PMC_ACPRESENT D20 (+V1P8A) PMC_ACPRESENT R236 2K20 +V1P8A
PMC_WAKE_PCIE_0 F26 (+V1P8A) PMC_PCIE_WAKE_R V.B - Added PU R253 1K00 +V1P8A
PMC_BATLOW K26 (+V1P8A) PMC_BATLOW R256 20K0 +V1P8A
PMC_PWRBTN J26 (+V1P8A) PMC_PWRBTN
PMC_RSTBTN BG9 (+V1P8S)
PMC_PLTRST F20 (+V1P8A) PMC_RSTBTN 17
J24 PMC_PLTRST_R_V1P8 17
GPIO_S5_17 G18 (+V1P8A) LPCPD_L TP7
PMC_SUS_STAT

R82 100K GND
PMC_RSMRST
RC delay >10us
R83 10K0 +3VSB
C49 10pF GND

ILB_RTC_TEST C11 (+RTCVCC) ILB_RTC_TESTB 17
PMC_RSMRST 17,22

PMC_RSMRST B10 (+RTCVCC) PMC_RSMRST
PMC_CORE_PWROK B7 (+RTCVCC) PMC_CORE_PWROK
PMC_CORE_PWROK 17
DNI C33 1.0uF GND
R59 0R0 SYS_PWRGD 4,26

ILB_RTC_X1 C9 (+RTCVCC) BRTCX1
ILB_RTC_X2 A9 (+RTCVCC) BRTCX2
ILB_RTC_EXTPAD B8 (+RTCVCC) BVCCRTC_EXTPAD C41 0.1uF GND

R104 69R8 +V1P0S
2013/7/11 Intel Require
R76 10M0
Y1 32.768KHz, ABRACON
C42 18pF C43 18pF CL=12.5pF GND

SVID_ALERT B24 (+V1P0S) SVID_ALERT R100 20R0 SVID_ALERT-R 23
SVID_DATA A25 (+V1P0S) SVID_DATA R101 16R9 SVID_DATA-R 23
SVID_CLK C25 (+V1P0S) SVID_CLK SVID_CLK-R 23

SIO_PWM_00 AU32 SOC_PWM0 20
SIO_PWM_11 AT32 SOC_PWM1 20
(+V1P8A)

UPDATE Y1 SYMBOL

GPIO_S5_22 K24 (+V1P8A)
GPIO_S5_23 N24 (+V1P8A) XDP_H_OBSDATA_A0 17
GPIO_S5_24 M20 (+V1P8A) XDP_H_OBSDATA_A1 17
GPIO_S5_25 J18 (+V1P8A) XDP_H_OBSDATA_A2 17
GPIO_S5_26 M18 (+V1P8A) XDP_H_OBSDATA_A3 17
GPIO_S5_27 K18 (+V1P8A) EXP_GPIO1 17
GPIO_S5_28 K20 (+V1P8A) EXP_GPIO2 17
GPIO_S5_29 M22 (+V1P8A) EXP_GPIO3 17
GPIO_S5_30 M24 (+V1P8A) EXP_GPIO4 17

Bay Trail-M Remove SPI port
SIO_SPI_CS AV32 (+V1P8S) SOC_SIO_SPI_CS1 20
SIO_SPI_MISO BA28 (+V1P8S) SOC_SIO_SPI_MISO 20
SIO_SPI_MOSI AY28 (+V1P8S) SOC_SIO_SPI_MOSI 20
SIO_SPI_CLK AY30 (+V1P8S) SOC_SIO_SPI_CLK 20

+PS_3VSB +RTCVCC
R279 20K0 RTCRST_L
C286 1.0uF D5 BAT54C-S C285 1.0uF GND

UPDATE D5 SYMBOL

+VBAT DNI R278 2+VBAT_R 1K00
VBAT Circuit
DNI BH1 BATT HOLDER, BS-1225-PC GND
DNI BAT1 COIN BATTERY, BR-1225

+3VSB C15 0.1uF
+V1P8A GND C32 0.1uF DNI
U7 TXS0104EYZT
VCCA VCCB OE GND
PMC_SLP_S3_L PMC_SLP_S4_L PMC_SUSCLK0 PMC_PLTRST_R_V1P8 PMC_OE
R58 2K20 R57 2K20
PWR_BUF1 R26 0R0
R53 2K20 R54 2K20 R55 10K0 R56 2K20
SLP_S3_L 22,25,26
SLP_S4_L 22,25
SUSCLK_3P3
PMC_PLTRST_L 18

Level Shifter

PMC_PCIE_WAKE_R D3 BAT54A-S R27 2K20 PMC_PCIE_WAKE 18

UPDATE
D10 SYMBOL

+V1P8A +3VSB
DNI R161 20K0 R162 1K00
PWRBTN PMC_PWRBTN
3VSB_OK D10 BAT54C-S PS_OUT_L 22

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MINNOWBOARD2 - CPU-SPI/CLOCK/RTC/PMC/UART

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Bay Trail-I USB_ULPI Port

CPU1F — INTEL ATOM 3825 PROCESSOR

(+V1P8A) G2 GPIO_S5_31

(+V1P8A) M3 GPIO_S5_32
(+V1P8A) L1 GPIO_S5_33
(+V1P8A) K2 GPIO_S5_34
(+V1P8A) K3 GPIO_S5_35
(+V1P8A) M2 GPIO_S5_36
(+V1P8A) N3 GPIO_S5_37
(+V1P8A) P2 GPIO_S5_38
(+V1P8A) L3 GPIO_S5_39

(+V1P8A) J3 GPIO_S5_40
(+V1P8A) P3 GPIO_S5_41
(+V1P8A) H3 GPIO_S5_42
(+V1P8A) B12 GPIO_S5_43

RESERVED_M10 M10
RESERVED_M9 M9
RESERVED_P7 P7
RESERVED_P6 P6
RESERVED_M7 M7
USB3_REXT0 M12 (+V1P0A) USB3_REXT0 — R212 1 2 1K24 — GND
RESERVED_P10 P10
RESERVED_P12 P12
RESERVED_M4 M4
RESERVED_M6 M6

USB3_RXP0 D4 (+V1P0A) — USB3_RXP0 16
USB3_RXN0 E3 (+V1P0A) — USB3_RXN0 16
USB3_TXP0 K6 (+V1P0A) — USB3_TXP0 16
USB3_TXN0 K7 (+V1P0A) — USB3_TXN0 16

USB3 HIGH SPEED TX and RX LINES

USB3.0

16 USB_DP0 — (VUSB2) M16 — USB_DP0
16 USB_DN0 — (VUSB2) K16 — USB_DN0

USB2.0

16 USB_DP1 — (VUSB2) J14 — USB_DP1
16 USB_DN1 — (VUSB2) G14 — USB_DN1

mPCIE USB CHANNEL

17 USB_HOST_DP — (VUSB2) K12 — USB_DP2
17 USB_HOST_DN — (VUSB2) J12 — USB_DN2

(VUSB2) K10 USB_DP3
(VUSB2) H10 USB_DN3

RESERVED_H8 H8
RESERVED_H7 H7
RESERVED_H5 H5
RESERVED_H4 H4

GND — R187 1 2 1K00 ICLK_USB_TERM_0 — D10 ICLK_USB_TERM_1
R186 1 2 1K00 ICLK_USB_TERM_1 — F10 ICLK_USB_TERMN

+V1P8A — R84 10K0 — (+V1P8A) C20 USB_OC_00
16 SOC_USB_HOST_OC0 — B20 USB_OC_11
+V1P8A — R97 10K0 — (+V1P8A)
16 SOC_USB_HOST_OC1

GND — R185 1 2 45R3 — USB_RCOMP — D6 USB_RCOMPO, C7 USB_RCOMPI

TP3 — USB_PLL_MON — M13 USB_PLL_MON

(+V1P24A) B4 USB_HSIC0_DATA
(+V1P24A) B5 USB_HSIC0_STROBE

(+V1P24A) E2 USB_HSIC1_DATA
(+V1P24A) D2 USB_HSIC1_STROBE

GND — R77 1 2 45R3 — USB_HSIC0_RCOMP — (+V1P24A) A7 USB_HSIC_RCOMP

GND — R241 2 1 49R9 — LPC_RCOMP — (+VLPC) BF18 LPC_RCOMP

(+VLPC) BH16 ILB_LPC_AD_00
(+VLPC) BJ17 ILB_LPC_AD_11
(+VLPC) BJ13 ILB_LPC_AD_22
(+VLPC) BG14 ILB_LPC_AD_33
(+VLPC) BG17 ILB_LPC_FRAME
(+VLPC) BG15 ILB_LPC_CLK_00
(+VLPC) BH14 ILB_LPC_CLK_11
(+VLPC) BG16 ILB_LPC_CLKRUN
(+VLPC) BG13 ILB_LPC_SERIRQ

8 PCU_SMB_DATA — PCU_SMB_DATA — (+V1P8S) BG12 PCU_SMB_DATA
8 PCU_SMB_CLK — PCU_SMB_CLK — (+V1P8S) BH10 PCU_SMB_CLK
+V1P8S — R75 10K0 — PCU_SMB_ALERT — (+V1P8S) BG11 PCU_SMB_ALERT

GPIO_S0_SC_55 BD12 (+V1P8S) GPIO_S0_SC_55 — TP8
GPIO_S0_SC_56 BC12 (+V1P8S) GPIO_S0_SC_56 6
GPIO_S0_SC_57 BD14 (+V1P8S)
GPIO_S0_SC_58 BC14 (+V1P8S) GPIO_S0_SC_58 — TP9
GPIO_S0_SC_59 BF14 (+V1P8S) HDMI_DCDC_ENB 15
GPIO_S0_SC_60 BD16 (+V1P8S) HDMI_LDSW_ENB 15
GPIO_S0_SC_61 BC16 (+V1P8S)

ILB_8254_SPKR BH12 (+V1P8S) ILB_8254_SPKR 20

SIO_I2C0_DATA BH22 (+V1P8S)
SIO_I2C0_CLK BG23 (+V1P8S)

SIO_I2C1_DATA BG24 (+V1P8S) SIO_I2C1_SDA — TP6
SIO_I2C1_CLK BH24 (+V1P8S) SIO_I2C1_SCL — TP5

SIO_I2C2_DATA BG25 (+V1P8S)
SIO_I2C2_CLK BJ25 (+V1P8S)

SIO_I2C3_DATA BG26 (+V1P8S)
SIO_I2C3_CLK BH26 (+V1P8S)

SIO_I2C4_DATA BF27 (+V1P8S)
SIO_I2C4_CLK BG27 (+V1P8S)

SIO_I2C5_DATA BH28 (+V1P8S) SI0_I2C5_SDA — R269 1 2 22R0 — I2C5_SDA 20
SIO_I2C5_CLK BG28 (+V1P8S) SI0_I2C5_SCL — R270 1 2 22R0 — I2C5_SCL 20

SIO_I2C6_DATA BJ29 (+V1P8S) SI0_I2C6_SDA — R11 1 2 22R0 — I2C6_SDA 17
SIO_I2C6_CLK BG29 (+V1P8S) SI0_I2C6_SCL — R12 1 2 22R0 — I2C6_SCL 17

GPIO_S0_SC_092 BH30 (+V1P8S) TP13 TP9_NET — R243 1 2 0R0 — GND
GPIO_S0_SC_093 BG30 (+V1P8S) TP16 TP10_NET — R261 1 2 0R0 — GND

GROUNDING THESE PINS THROUGH 0 OHM RESISTORS

REWORK
CHANGE NAME FROM LSS_I2C_SCL/SDA to I2C5_SCL/SDA

LOW SPEED SERIAL I2C BUS

EXPANSION I2C BUS

REWORK
CHANGE NAME FROM EXP_I2C_SCL/SDA to I2C6_SCL/SDA

UPDATE
J4 SYMBOL - PCB FOOTPRINT ADJUST
PIN1 - ID - BIG MARK
PIN1 REF - PHYSICALLY TURN AROUND HEADER

+V1P8S — 0.1uF C30 — GND
U6: C1, C2, D1, D2, VCCA, VCCB, A1, A2, B1, B2, OE, GND — TXS0102YZP
PCU_UART3_RXD D2 — BUF3_PWR B2
PCU_UART3_TXD D1 — DBG_UART3_RXD A2
LSENB C2 — DBG_UART3_TXD A1
+V1P8S — 2K20 R52 — LSENB
BUF3_PWR — R51 1 2 0R0
GND — C31 0.1uF — +3VSB
GND — R50 100K — GND

Mark pin 1 clearly
UART3 Serial Port
J4: 1 2 3 4 5 6 — SIP6_RA
USB to TTL Serial Cable 3.3V

BAYTRAIL_I
REV = 1.0
6 OF 13

GPIO_USB_ILB_I2C_SECTION

+V1P8S — GND — C29 0.1uF
2K20 R49
2K20 R45
2K20 R177
+VCC3 — 0.1uF C14 — GND
2K20 R44
2K20 R47
U5: C1, C2, D1, D2, VCCA, VCCB, A1, A2, B1, B2, OE, GND — TXS0102YZP
8 PCU_SMB_DATA — PCU_SMB_DATA
8 PCU_SMB_CLK — PCU_SMB_CLK
PCU_SMB_BUFF_ENB
BUF2_PWR — R48 1 2 0R0
DDR_SMB_DATA
DDR_SMB_CLK
DDR_SMB_DATA 12,22
DDR_SMB_CLK 12,22

LEVEL SHIFTER LOGIC

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MINNOWBOARD2 - CPU-USB/LPC/SMB/I2C

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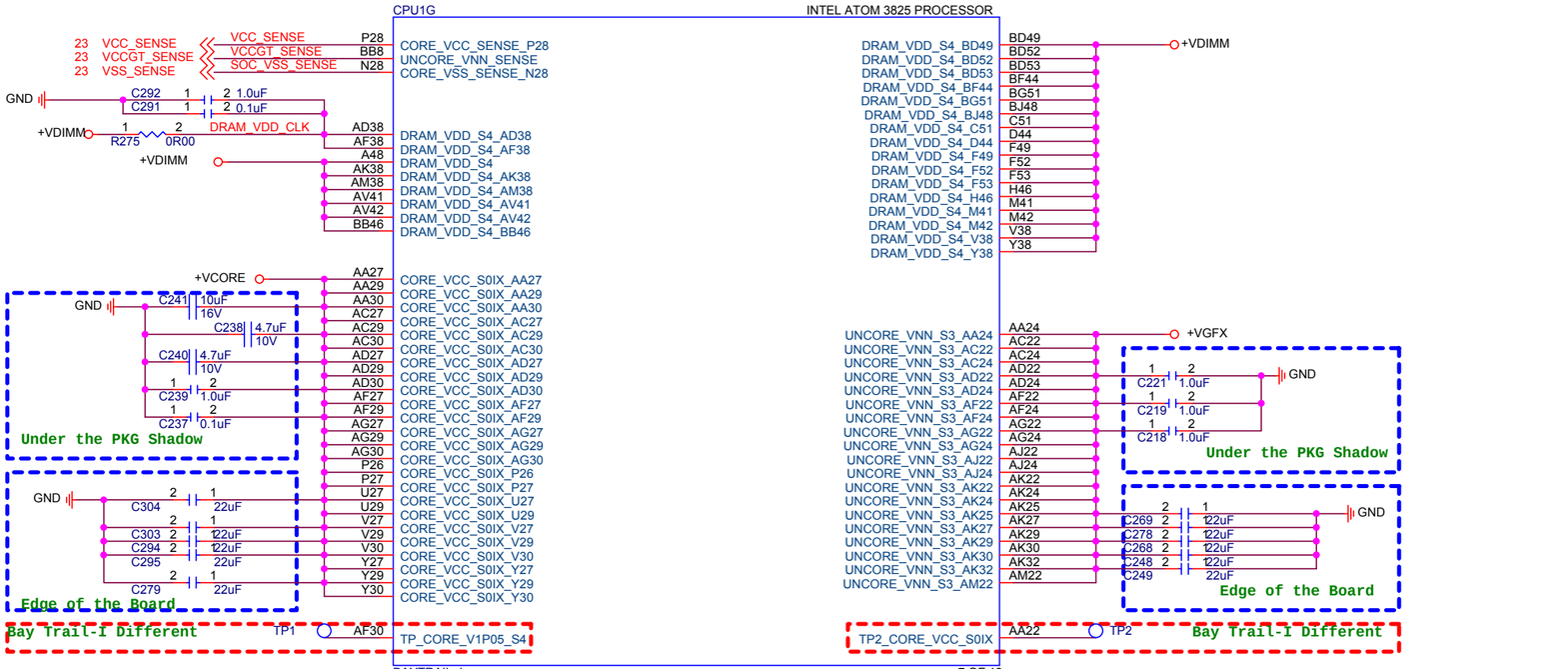

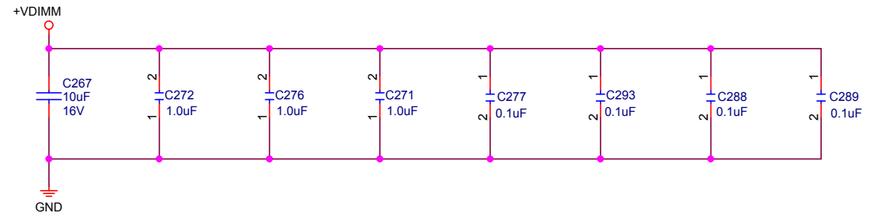

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MINNOWBOARD2 - CPU-PWR1/TPM/LPC

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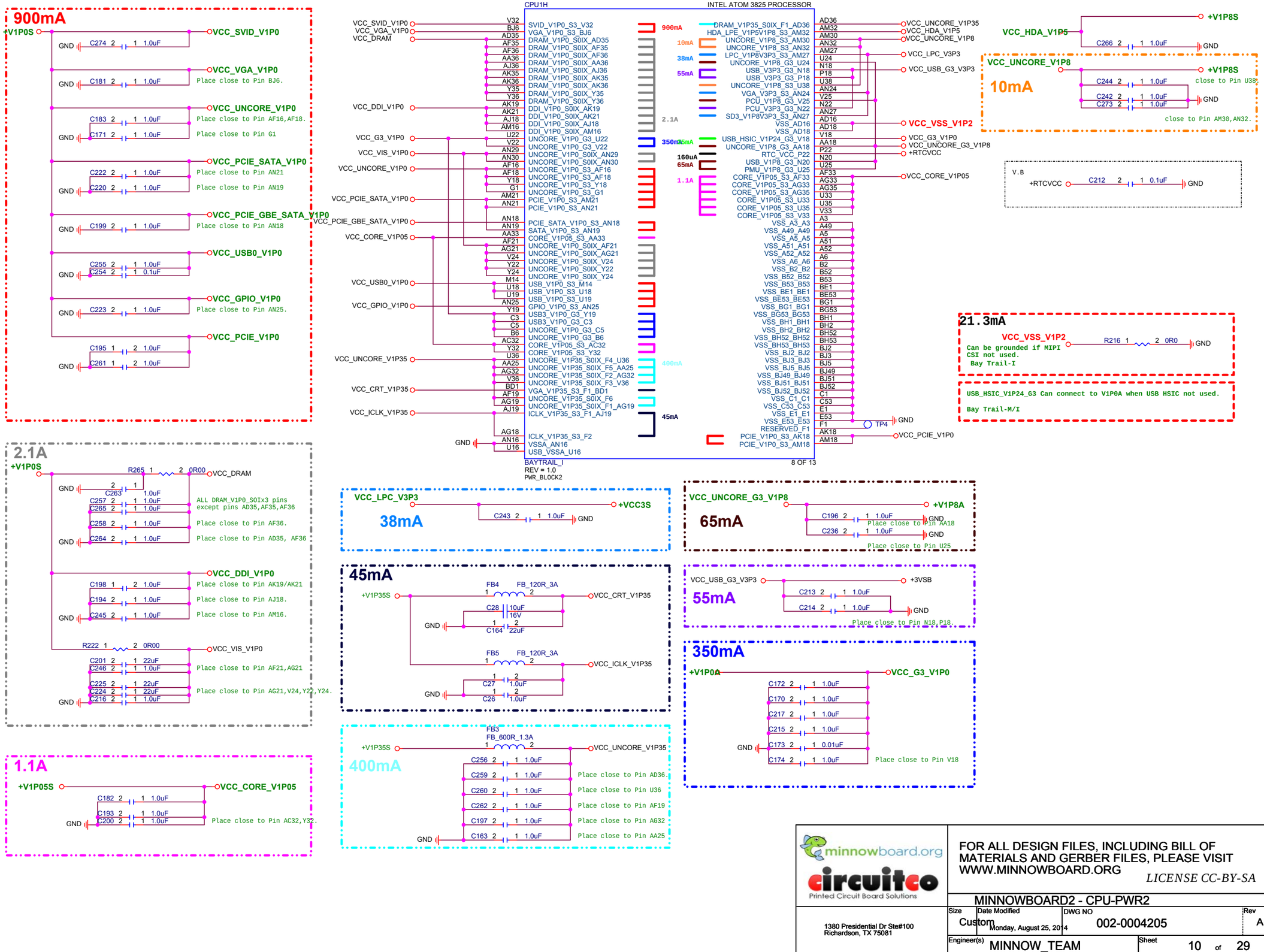

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MINNOWBOARD2 - CPU-PWR2

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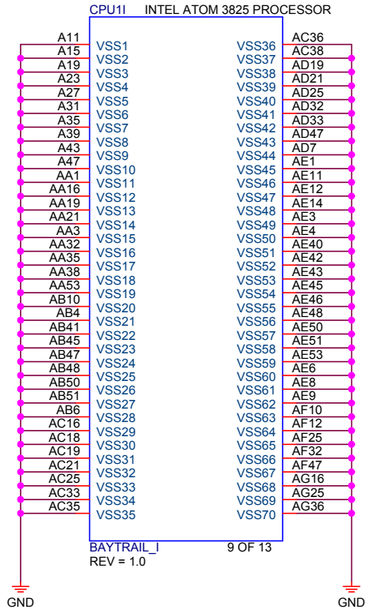
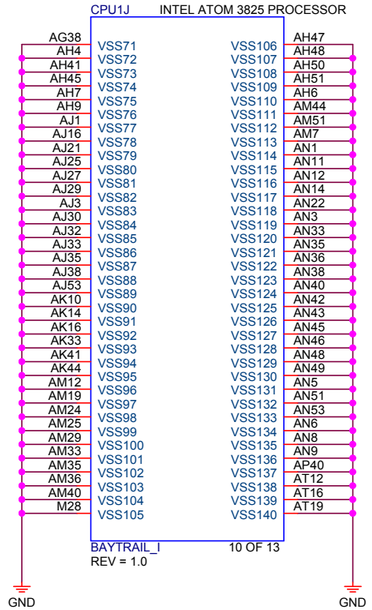
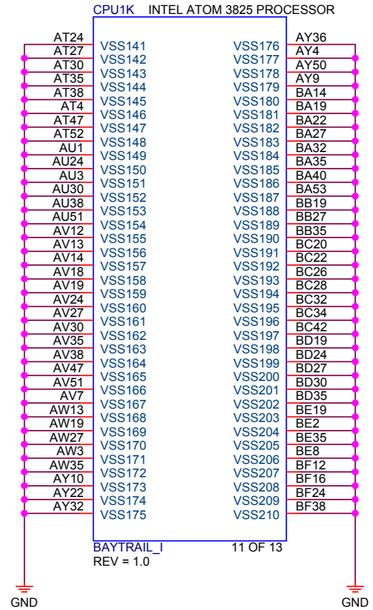
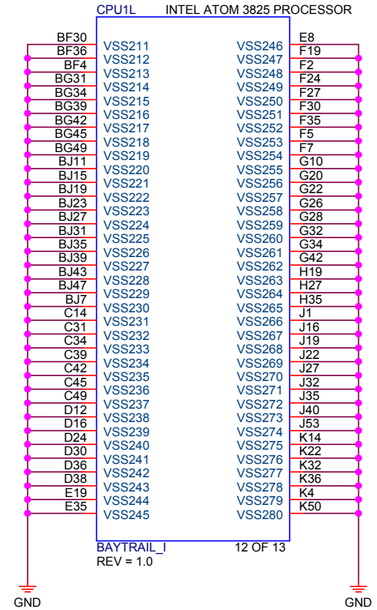
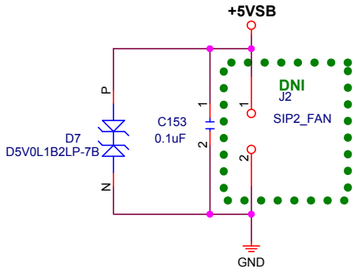


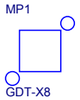






REWORK
TURN AROUND C153 & J2
PINOUT PIN1=5V





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MINNOWBOARD2 - CPU-GND

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UPDATE MEM2 SYMBOL - 256Mx16

UPDATE CAP SYMBOLS

MEM2

256M*16

MICRON MT41K256M16HA

Swap Circuit

UPDATE MEM3 SYMBOL - 256Mx16

MEM3

256M*16

MICRON MT41K256M16HA

Swap Circuit

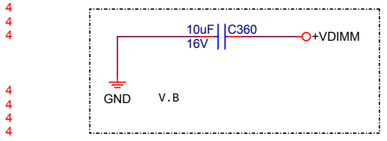
NOTE: COMPATIBLE DDR3L MEMORIES FOR THE MINNOWMAX ARE THE FOLLOWING: MICRON MT41K128M16HA-125:D, MICRON MT41K256M16HA-125:E, MICRON MT41K512M16TNA-125:X

Modify to 1% 4.7K Ohm.

Add R/C for DRAMRST.

M24C02-WMN6TP-X

Size:2K



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MINNOWBOARD2 - Memory_CHA-1

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UPDATE MEM1 SYMBOL - 256Mx16

UPDATE CAP SYMBOLS

UPDATE MEM4 SYMBOL - 256Mx16

UPDATE 36R0 SYMBOLS

MEM1

MEM4

256M*16

MICRON MT41K256M16HA

Swap Circuit

NOTE: COMPATIBLE DDR3L MEMORIES FOR THE MINNOWMAX ARE THE FOLLOWING: MICRON MT41K128M16HA-125:D, MICRON MT41K256M16HA-125:E, MICRON MT41K512M16TNA-125:X

Modify to 1% 4.7K Ohm.

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MINNOWBOARD2 - Memory_CHA-2

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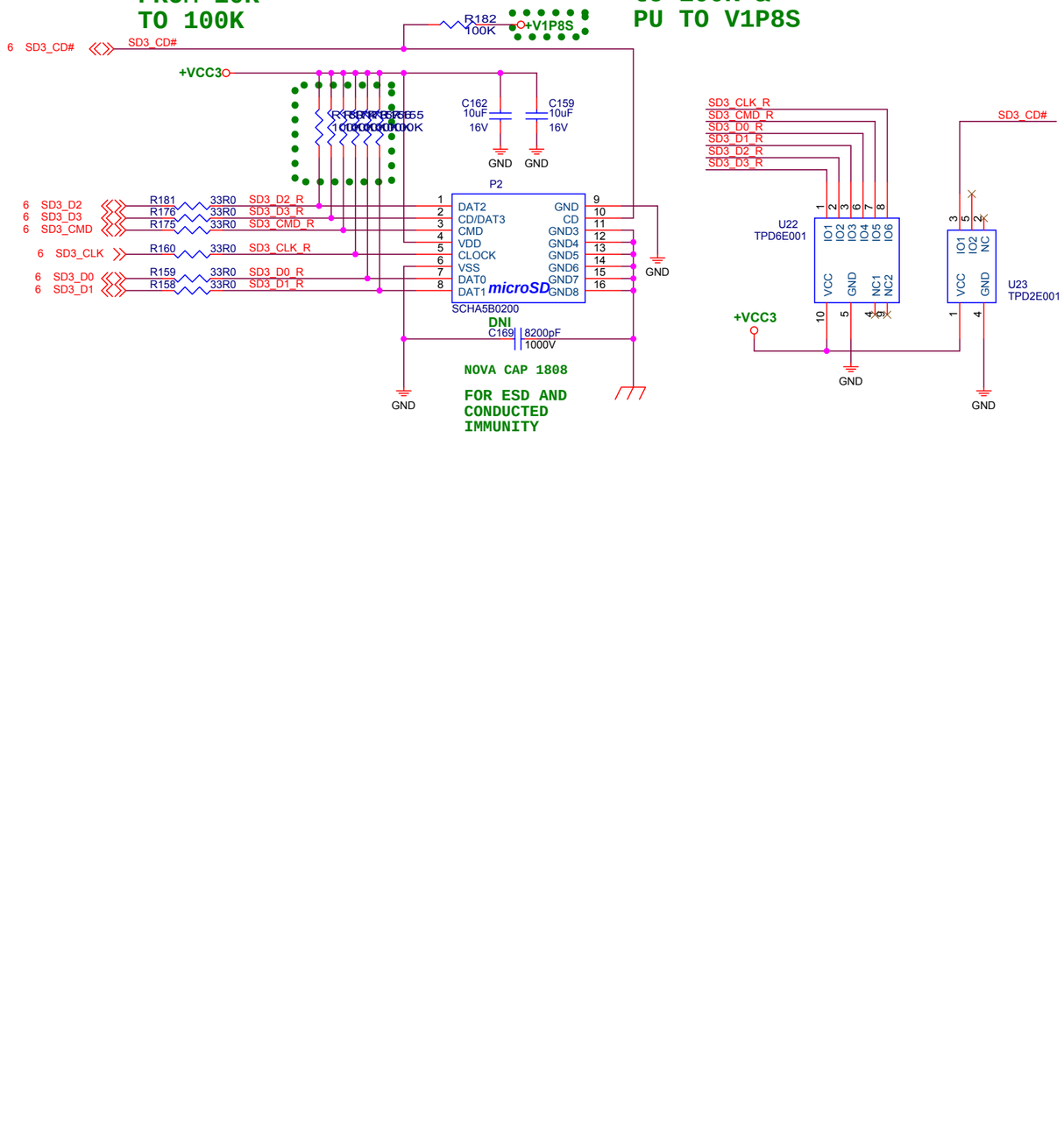
REWORK -
R180,R174,R173,
R157,R156,R155
CHANGE
FROM 10K
TO 100K

REWORK -
R182
CHANGE
to 100K &
PU TO V1P8S



MINNOWBOARD2 - uSD CARD CAGE

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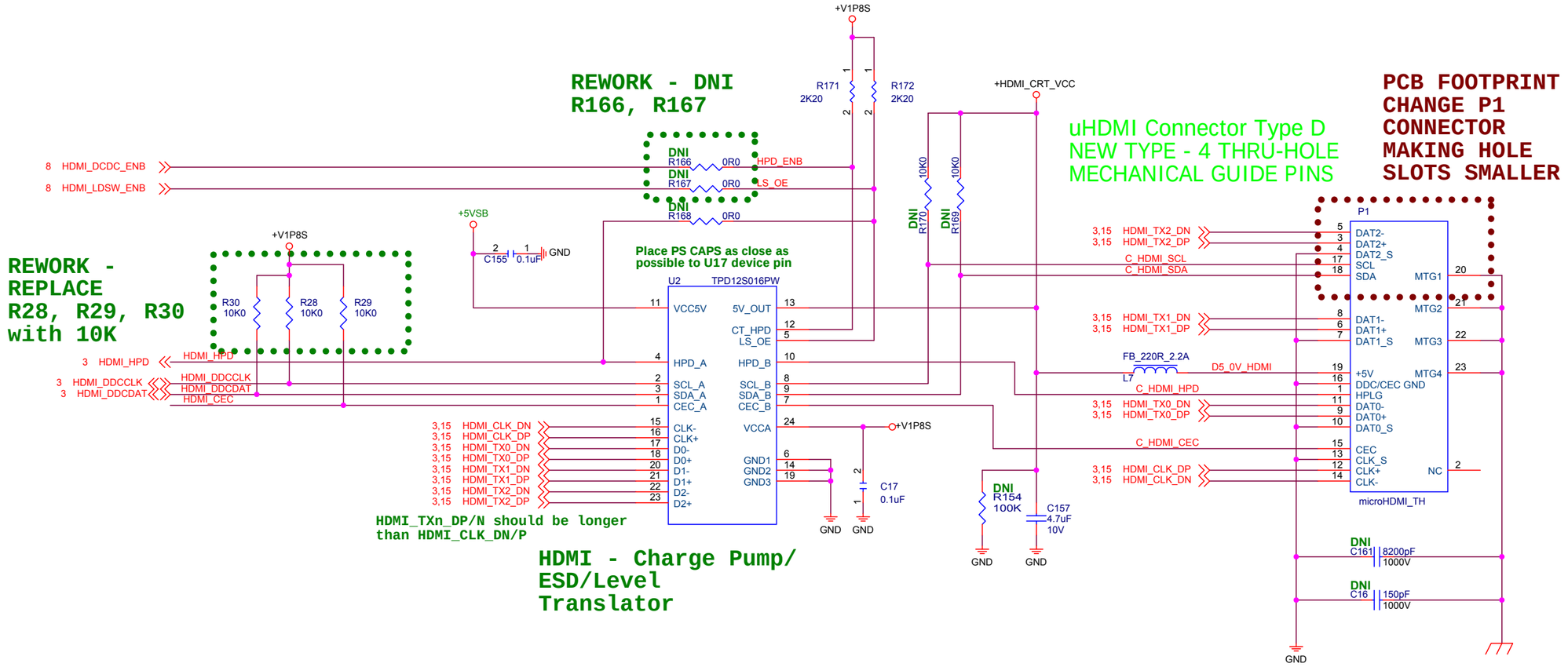

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MINNOWBOARD2 - uHDMI

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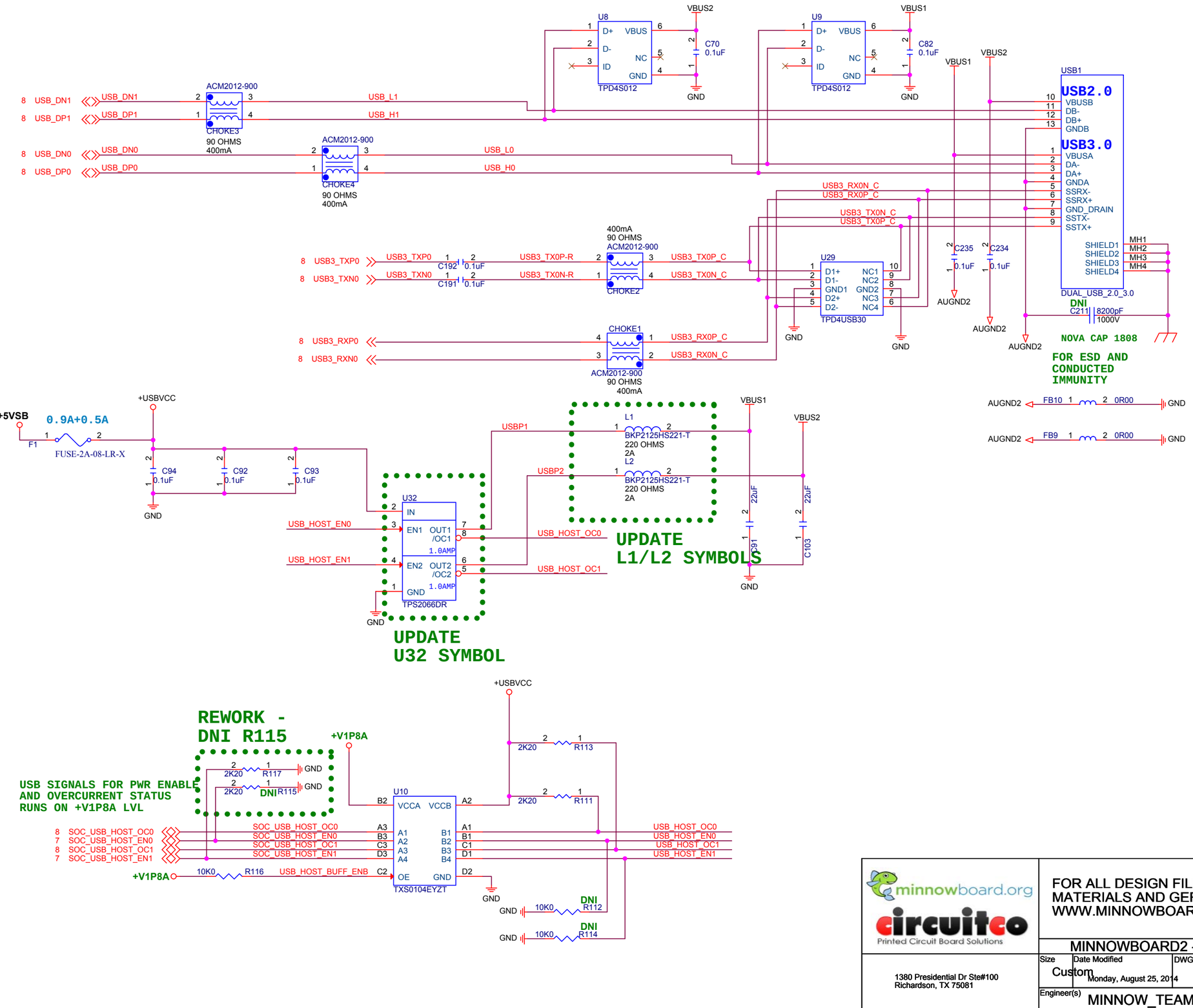

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MINNOWBOARD2 - USB3+USB2

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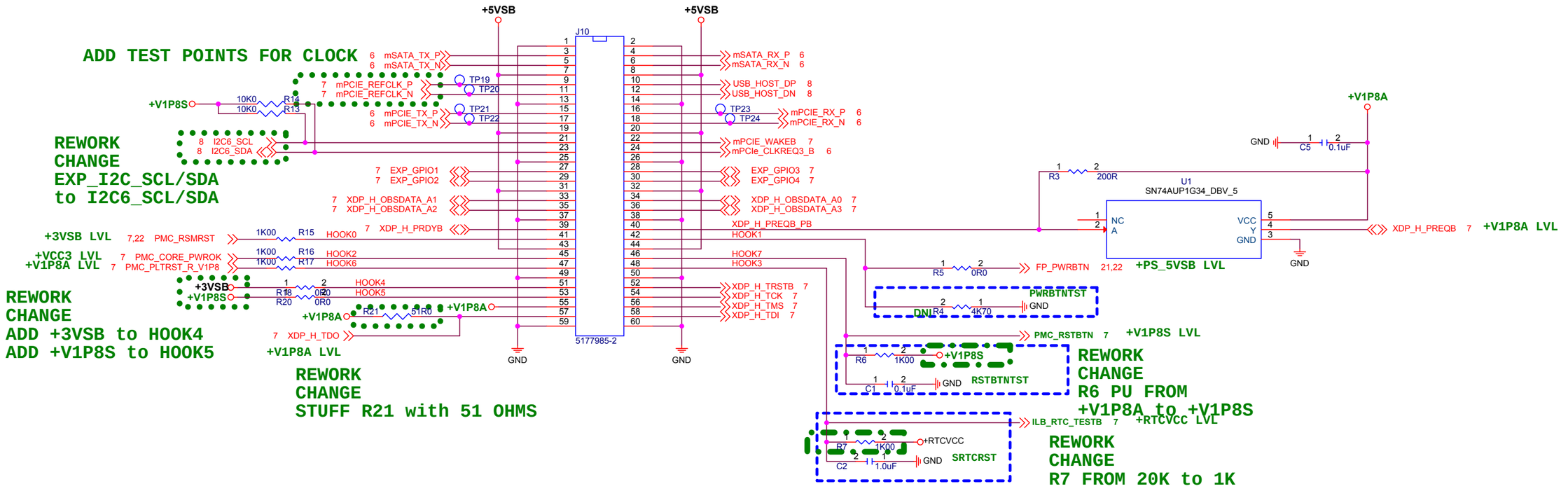
EXPANSION HS CONNECTOR WITH mPCIE, mSATA, I2S AUDIO, GPIO, and XDP I/O



MINNOWBOARD2 - EXPANSION CONNECTOR I/O

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for EMI

ACTIVE-LED DNI C231 2 1 0.1uF
LINK-LED DNI C209 2 1 0.1uF
LINK-GIGALED DNI C166 2 1 0.1uF
GND

+3VSB 3VSB
+VCC3 VCC3
AUGND2 AUGND2

Ch

AVDDREG C230 10uF 16V GND
Closed To Pin 23

VDD1.0 C251 10uF 16V GND
Closed To The CHOKE¡I

UPDATE Y3 SYMBOL - 25MHz

GND C252 2 1 27pF LAN_XTAL1
GND
GND C253 2 1 27pF LAN_XTAL2
Y3 25.00MHz
R264 1M00
L_XTAL1
L_XTAL2
1 R105 2 2K49 LAN_RSET
3VSB VDD1.0

LAN_ACTIVE- R106 1 2 330R ACTIVE-LED
LED1-LINK R107 1 2 0R0 LINK-LED
LED2-LINK R108 1 2 0R0 LINK-GIGALED

LAN1
33 GND
GND
32 AVDD33
31 RSET
30 AVDD10
29 CKXTAL2
28 CKXTAL1
27 LED0
26 LED1/GPO
25 LED2(LED1)

MDI_P0 1 MDIP0
MDI_N0 2 MDIN0
3 AVDD10(NC)
VDD1.0
MDI_P1 4 MDIP1
MDI_N1 5 MDIN1
MDI_P2 6 MDIP2(NC)
MDI_N2 7 MDIN2(NC)
8 AVDD10_1

REALTEK

24 REGOUT(NC) REGOUT
23 VDDREG(VDD33) AVDDREG
22 DVDD10(NC)
21 LANWAKEB
20 ISOLATEB ISOLATEB
19 PERSTB
18 HSON HSON C205 1 2 0.1uF
17 HSOP HSOP C206 1 2 0.1uF

Cg
For SNR Over 75%
L8 1 2 IND-4.7U-S-X
VDD1.0
FB8 1 2 0R00 3VSB
PMC_PCIE_WAKE 7
PMC_PLTRST_L 7
PCIE_RXN2 6
PCIE_RXP2 6

ISOLATION PIN
WAIT FOR SYSTEM
POWER UP
R78 1 2 1K00
DNI R79 1 2 15K
VCC3

9 MDIP3(NC)
10 MDIN3(NC)
11 AVDD33(NC)
12 CLKREQB
13 HSIP
14 HSIN
15 REFCLK_P
16 REFCLK_N

MDI_P3
MDI_N3
3VSB
VCC3
DNI R231 10K0 LAN_CREQ
R232 1 2 0R0
6 LAN_CLKREQ2_B

ADD TP17/TP18 FOR CLK OBSERVATION
TP17
TP18
PCIE_CLK-N2 7
PCIE_CLK-P2 7
HSIN C207 1 2 0.1uF PCIE_TXN2 6
HSIP C208 1 2 0.1uF PCIE_TXP2 6

OVERLAP SR82 and SR106 so ONLY 1
RESISTOR CAN BE INSTALLED AT A TIME.

Ca
RTL8111GS-CG-X

8106E : NC PIN - 3,6,7,9,10,11,22,24

VDD1.0
Closed To Pin 3, 8, 22, 24, 30
C54 1 2 0.1uF
C56 1 2 0.1uF
C50 1 2 0.1uF
C58 1 2 0.1uF
C51 1 2 0.1uF
C57 1 2 1.0uF
GND
1U Close To Pin 22

3VSB
Closed To PIN 11, 23, 32
C55 1 2 0.1uF
C53 1 2 0.1uF
C52 1 2 0.1uF
C250 10uF 16V
GND

UPDATE J8
RJ-45 SYMBOL

DNI FB6 FB_120R_3A
ETH_CP
3VSB
J8
MDI_N0 DB0- 10
MDI_P0 DB0+ 9
MDI_N1 DB1- 8
MDI_P1 DB1+ 7
MDI_N2 DB2- 6
MDI_P2 DB2+ 5
MDI_N3 DB3- 4
MDI_P3 DB3+ 3
2
1
LED_LEFT D+ D1
D- D2
LED_RIGHT D+ D3
D- D4
RJ-45 Gigabit
MH1 MH2 SHELD1 SHELD2
DNI C233 8200pF 1000V
GND
DOUBLE VIA
NOVA CAP 1808

FOR ESD AND
CONDUCTED
IMMUNITY

3VSB
C167 0.1uF
GND
U25
LINK-GIGALED 2
4 LED_1000
SN74LVC1G14DBVR
1 3
GND
ACTIVE-LED
3VSB
C168 0.1uF
GND U26
1 2 3 5
4 ELL R207 220R LED_LEFT
74LVC1G08DBVR
GND

3VSB
C210 0.1uF
GND
U28
LINK-LED 2
4 LED_100_10
SN74LVC1G14DBVR
1 3
GND
ACTIVE-LED
3VSB
C232 0.1uF
GND U30
1 2 3 5
4 ELR R252 220R LED_RIGHT
74LVC1G08DBVR
GND

BOM Difference

	RTL8111GS-CG (SWR mode) 1000M	RTL8111G-CG (LDO mode) 1000M	RTL8106E-CG (LDO mode) 10/100M
Ca	RTL8111GS	RTL8111G	RTL8106E
Cb	None	None	None
Cc	USBX2-LAN-1000	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	X	V
Ce	0-04	0-04	.01U-25VX-04
Cf	V	V	X
Cg	L	R	X
Ch	V	X	X

DEFAULT

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MINNOWBOARD2 - LAN RT8111GS-CG

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MINNOWBOARD2 - AUDIO-ALC282

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SPI_PWR_FET_GATE
THICK ETCH
Q8
BSS138
+V1P8A
THICK ETCH
THICK ETCH
DDP_1V8
R163 10K0
R164 10K0
R165 10K0
C160 0.1uF
GND
U3
SPI_WP
SPI_HOLD
MICRON N25Q064A
GND
UPDATE U3 SYMBOL - N25Q064A 64M size
NOTE: COMPATIBLE U3 SPI ROM PARTS ARE THE FOLLOWING: MICRON N25Q032A, MICRON N25Q064A
U4
TS3A27518EZQS
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_CS0
COM1
COM2
COM3
COM4
COM5
COM6
/EN
IN1
IN2
N.C.
GND
V+
C165 0.1uF
NO1
NO2
NO3
NO4
NO5
NO6
NC1
NC2
NC3
NC4
NC5
NC6
SOC_SPI_CLK-R 7
SOC_SPI_MOSI-R 7
SOC_SPI_MISO-R 7
SOC_SPI_CS0B-R 7
DDP_SPI_CLK
DDP_SPI_MOSI
DDP_SPI_MISO
DDP_SPI_CS
At least 0.1" on the pin 1-2 side and the pin 7-8 side to allow space for the DediProg connector
REWORK - REPLACE R147 WITH 100K and PU to +3VSB
R152 10K0
J1
HEADER 4x2
DDP_SPI_CS
DDP_SPI_MISO
DDP_SPI_CLK
DDP_SPI_MOSI
DDP_IO3L
+3VSB
R147 100K
D8 BAT54C-S
UPDATE D8 SYMBOL
+V1P8S
+3VSB
U15
TXS0104EYZT
SOC_SIO_SPI_CS1
SOC_SIO_SPI_MISO
SOC_SIO_SPI_MOSI
SOC_SIO_SPI_CLK
SIO_SPI_CS1
SIO_SPI_MISO
SIO_SPI_MOSI
SIO_SPI_CLK
R338 10K0 LSS_OE2
U14
UART1_TXD
UART1_RXD
UART1_CTSB
UART1_RTSB
SIO_UART1_TXD 7
SIO_UART1_RXD 7
SIO_UART1_CTSB 7
SIO_UART1_RTSB 7
SIO_OE
R339 10K0
+5VSB
JP1
HDR-26
U17
SOC_UART2_TXD
SOC_UART2_RXD
UART2_TXD
UART2_RXD
R336 10K0 LSS_OE1
U16
I2SCLK_GPIO
I2SFRM_GPIO
I2SDO_GPIO
I2SDI_GPIO
I2S_CLK_R
I2S_FRM_R
I2S_DATOUT_R
I2S_DATIN_R
R127 0R0
R129 0R0
R130 0R0
R128 0R0
LPE_I2S_CLK 6
LPE_I2S_FRM 6
LPE_I2S_DATOUT 6
LPE_I2S_DATIN 6
LSS_OE5
R337 10K0
REWORK CHANGE NAME FROM LSS_I2C_SCL/SDA to I2C5_SCL/SDA
I2C5_SCL
I2C5_SDA
+V1P8A
+PS_3VSB
PICK THE ALWAYS ON 3.3V Power SUPPLY
U19
GPIO_S5_0
GPIO_S5_1
GPIO_S5_2
R334 10K0 LSS_OE3
U18
PWM0
PWM1
ILB_8254_GPIO
SOC_PWM0 7
SOC_PWM1 7
ILB_8254_SPKR 8
LSS_OE4
R335 10K0

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MINNOWBOARD2 - SPI PROM/LSS HEADER

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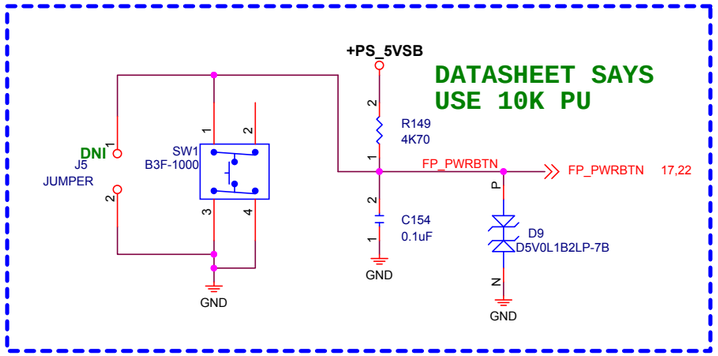
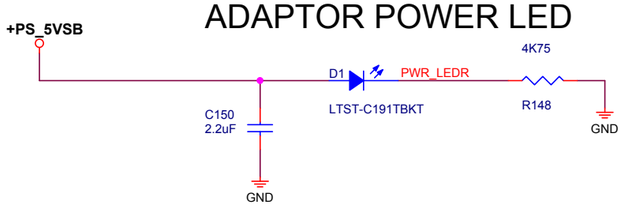
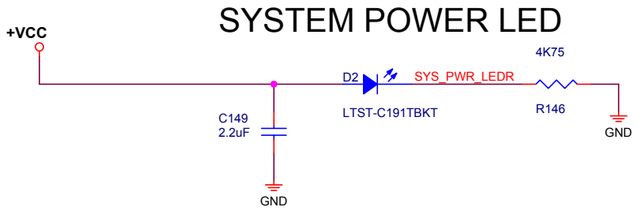
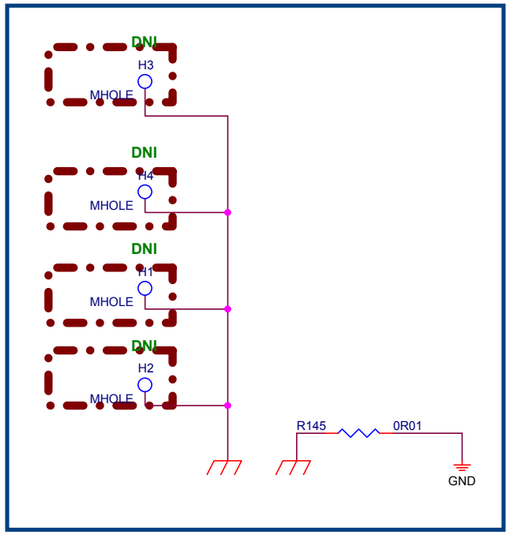






CHANGE MTG HOLES TO
6/32

BOARD HOLES - 4 TOTAL - 1 in EACH CORNER



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MINNOWBOARD2 - PWR BTN / LED / HOLES

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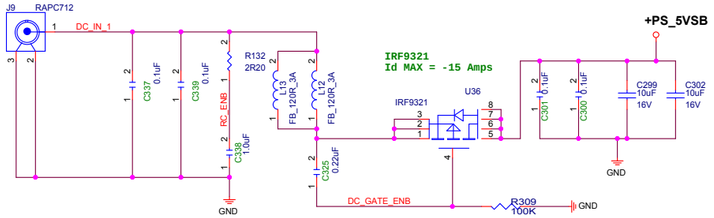
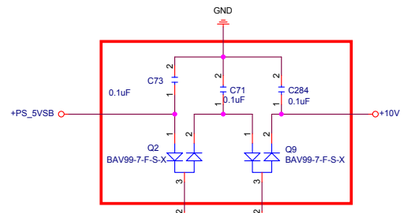
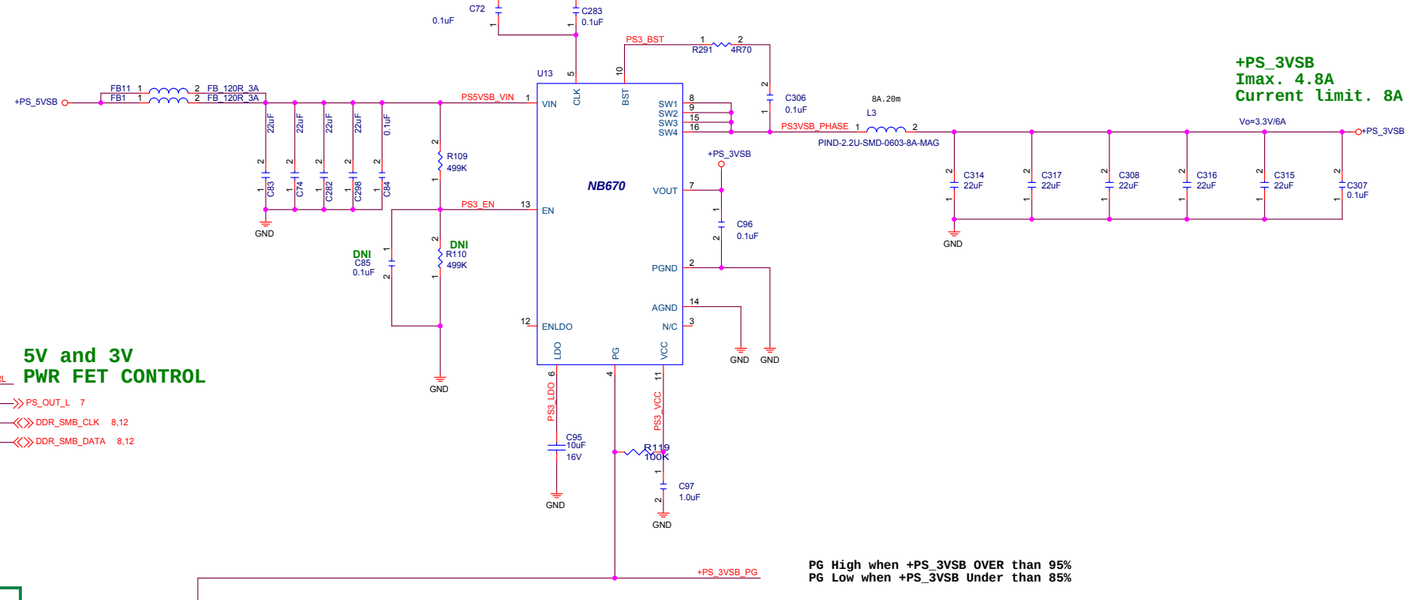
DC_IN 5V





+3.3VSB / Boost +10V



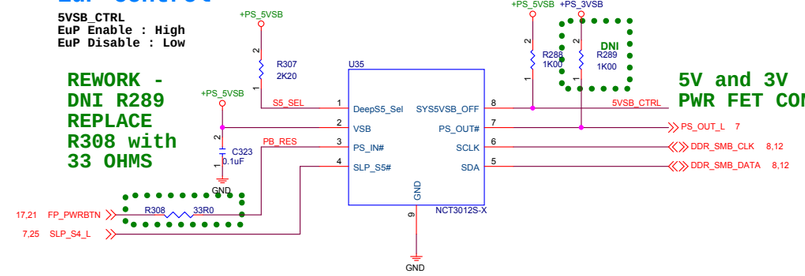
+PS_3VSB
Imax. 4.8A
Current limit. 8A

PG High when +PS_3VSB OVER than 95%
PG Low when +PS_3VSB Under than 85%

EuP Control

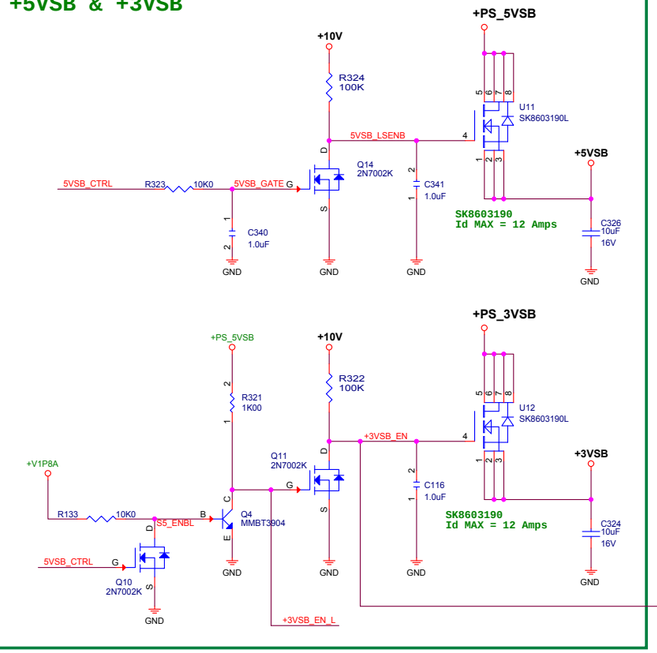
5VSB_CTRL
EuP Enable : High
EuP Disable : Low

REWORK -
DNI R289
REPLACE
R308 with
33 OHMS

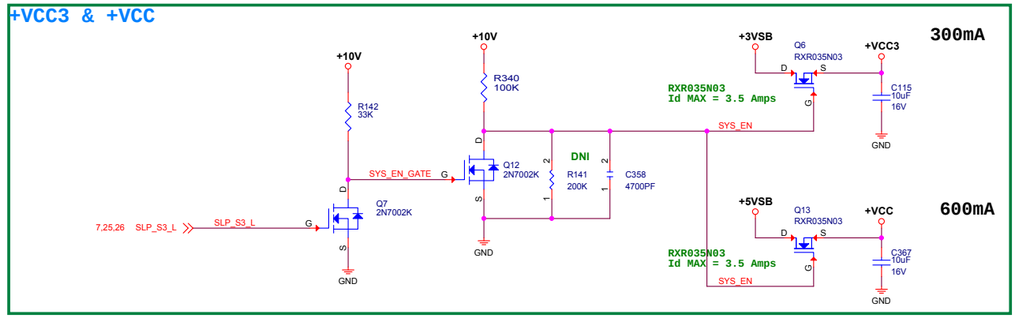


5V and 3V PWR FET CONTROL

+5VSB & +3VSB



+VCC3 & +VCC



+5V
+10V

VRTC LEVEL (+3VSB)

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MINNOWBOARD2 - DC-5VSB/3VSB / VCC / VCC3

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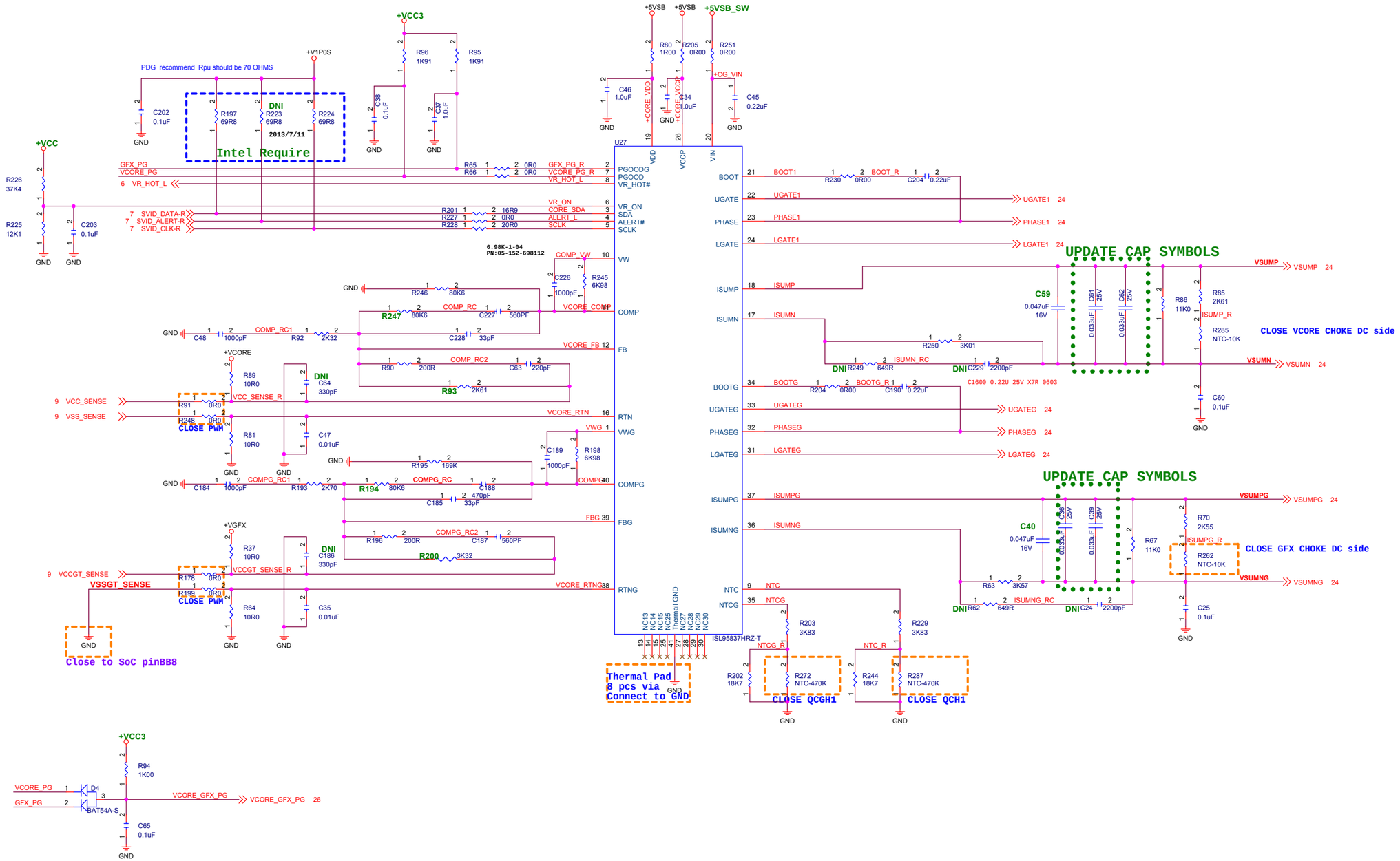

MINNOWBOARD2 - +5VSB/+3VSB

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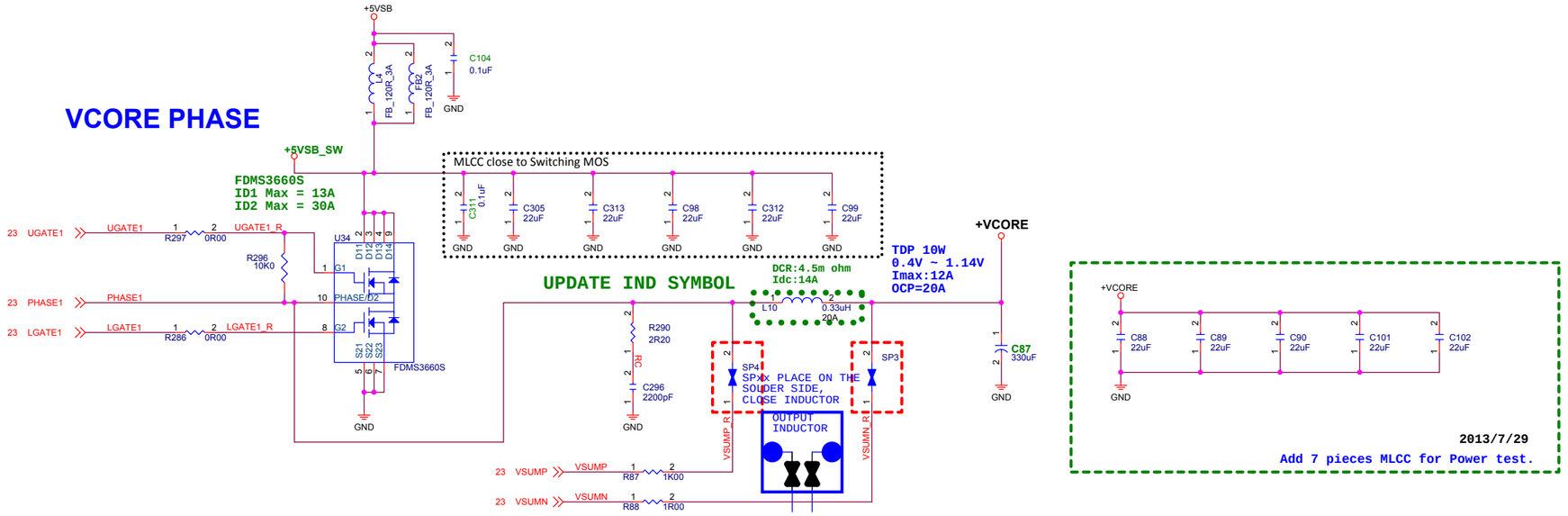
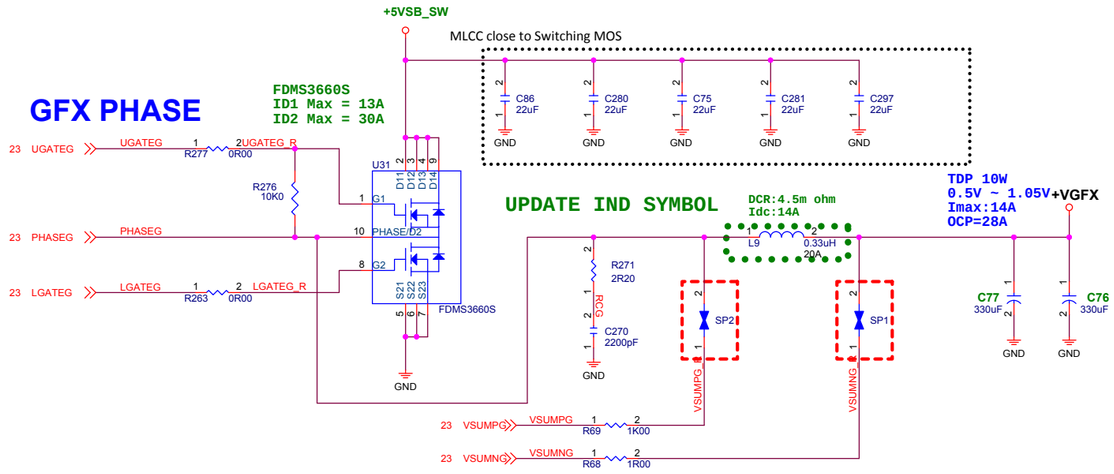
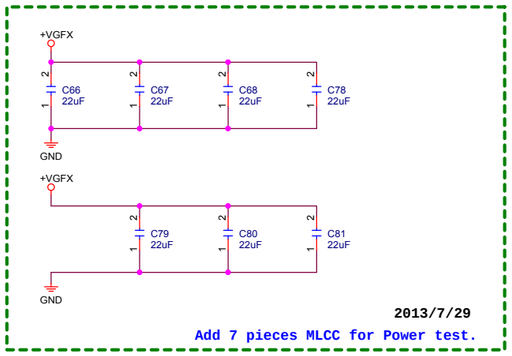
VCORE PHASE



GFX PHASE





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MINNOWBOARD2 - DC/DC VCORE/GFX MOS

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VDIMM

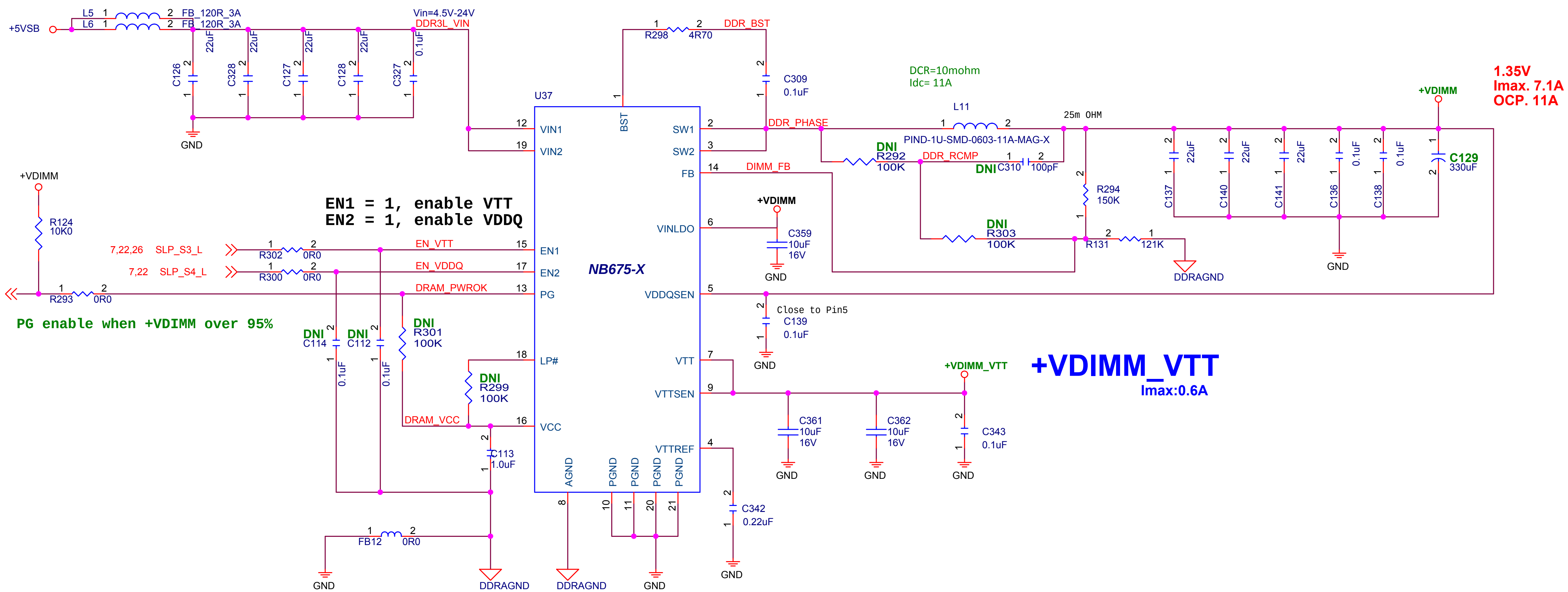
F= (Vin - 0.5) / 3.85p*Vin*Rton
Rton=806K , F=285KHz

on

on

RT8207M S3 and S5 truth table

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	on		on
S3	Lo	Hi	on		Off(Hi-Z)
S4/S5	Lo	Lo	Off Discharge	Off Discharge	Off Discharge



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MINNOWBOARD2 - DC-DIMM/DDR_VTT			
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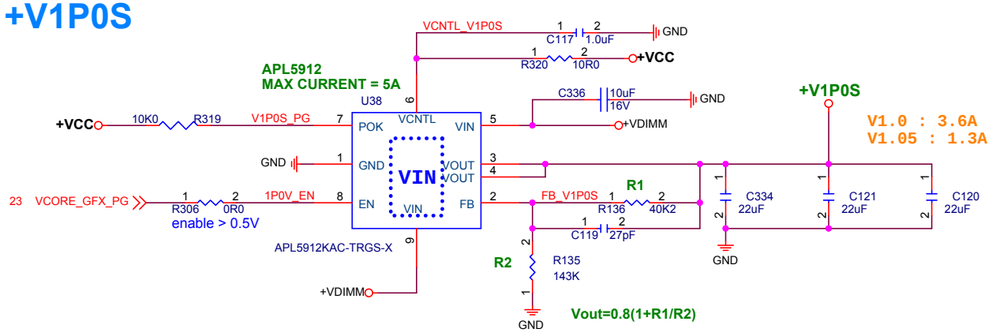
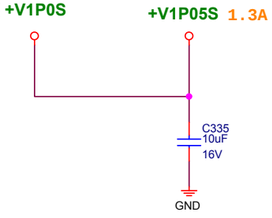
+V1P0S

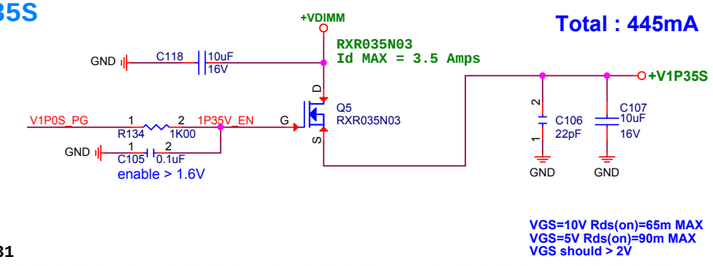


+V1P05S

Combine +V1P0S and +V1P05S

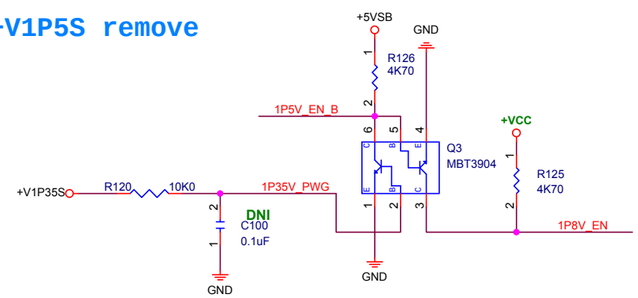


+V1P35S

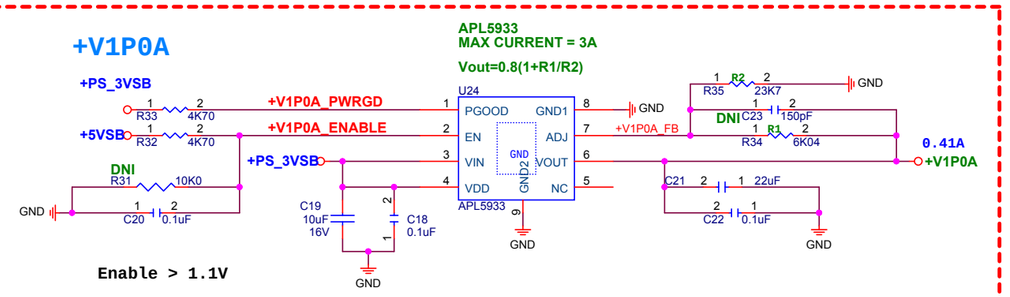


2013/7/31

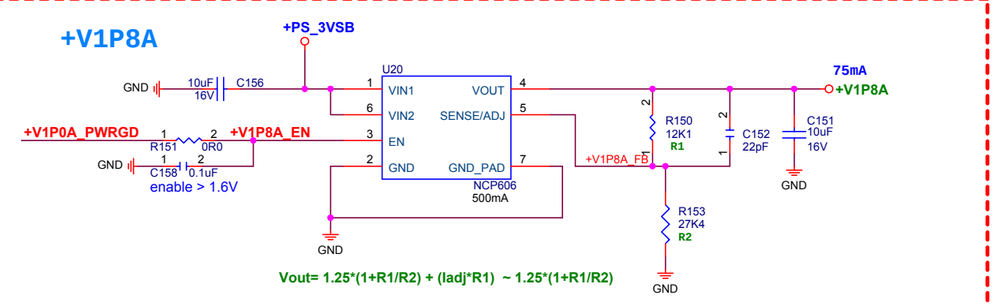
+V1P5S remove



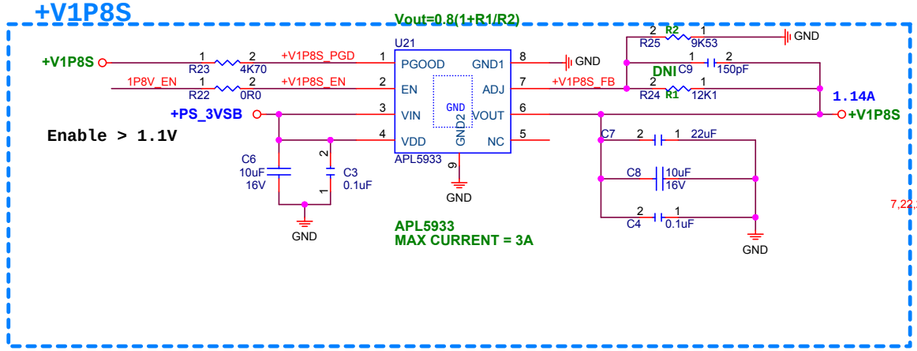
+V1P0A



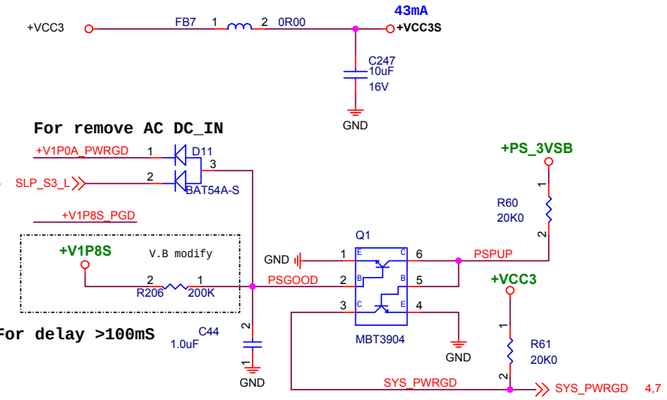
+V1P8A



+V1P8S



+VCC3S(For CPU)



MINNOWBOARD2 - DC-DC VOLTAGE

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PCH-GPIO function

Pin Name	Power Well	Usage	Boot Set
GPIO_S5[00]	1P8VSB, 20k,H	SOC_GPIO_S5_0 (LSS CONN)	GPO
GPIO_S5[01]	1P8VSB, 20k,H	SOC_GPIO_S5_1 (LSS CONN)	GPO
GPIO_S5[02]	1P8VSB, 20k,H	SOC_GPIO_S5_2 (LSS CONN)	GPO
GPIO_S5[03]	1P8VSB, 20k,H	mPCIE_WAKEB	GPI
GPIO_S5[04]	1P8VSB, 20k,L	OPEN	GPO
GPIO_S5[05]	1P8VSB, 20k,L	BOM OPTION	GPI
GPIO_S5[06]	1P8VSB, 20k,L	BOM OPTION	GPI
GPIO_S5[07]	1P8VSB, 20k,L	BOM OPTION	GPI
GPIO_S5[8]	1P8VSB, 20k,H	HDMI_DC_DC ENABLE	GPO
GPIO_S5[9]	1P8VSB, 20k,H	HDMI LD SWITCH ENABLE	GPO
GPIO_S5[10]	1P8VSB, 20k,H	TXE UNLOCK control	GPO
GPIO_S0_SC[022]	1P8V, 20k,H	OPEN	GPO
GPIO_S0_SC[023]	1P8V, 20k,H	XDP_H_OBSDATA_A0	GPO
GPIO_S0_SC[024]	1P8V, 20k,H	XDP_H_OBSDATA_A1	GPO
GPIO_S0_SC[025]	1P8V, 20k,H	XDP_H_OBSDATA_A2	GPO
GPIO_S0_SC[026]	1P8V, 20k,H	XDP_H_OBSDATA_A3	GPO
GPIO_S0_SC[027]	1P8V, 20k,H	EXPANSION_BUS GPIO1	GPO
GPIO_S0_SC[028]	1P8V, 20k,H	EXPANSION_BUS GPIO2	GPO
GPIO_S0_SC[029]	1P8V, 20k,H	EXPANSION_BUS GPIO3	GPO
GPIO_S0_SC[030]	1P8V, 20k,H	EXPANSION_BUS GPIO4	GPO
GPIO_S0_SC[058]	1P8V, 20k,L	GPIO reserved	GPO
GPIO_S0_SC[059]	1P8V, 20k,L	GPIO reserved	GPO
GPIO_S0_SC[060]	1P8V, 20k,L	GPIO reserved	GPO
GPIO_S0_SC[057]	1P8V, 20k,H	Debug Port UART3 TXD	UART
GPIO_S0_SC[061]	1P8V, 20k,H	Debug Port UART3 RXD	UART

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[056]	Legacy	1b	PMC_CORE_PWROK de-asserted	Top Swap (A16 Override) 0 = Top address bit is unchanged 1 = Top address bit is inverted
GPIO_S0_SC[063]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[065]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

Interrupt mapping

Function	INT# port	PCIe*1 port	Device
LAN	INTC#	port 2	RTL8111GS-CG

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MINNOWBOARD2 - GPIO/HW MAPPING

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DC-IN: +5V

+PS_5VSB

EuP

N-MOS

+5VSB
8A max

Switching

+10V (VOLTAGE DBLR)

+PS_3VSB
4.8A max

+3VSB

N-MOS

1.917A max

Switching

1.35V 7.1A max

0.075A @V1P8A
1.14A @V1P8S

LDO

1.8V 0.075A max

LDO

1.8V 1.14A max

0.3A max
+VCC3

N-MOS

0.6A max
+VCC

N-MOS

0.055A max

0.033A max

0.41A max

LDO

1.0V 410mA max

LDO

1.0V

LDO

1.05V

LDO

???? A max

0.75A max

1A max

0.2A max

0.07A max

??A max

1.4A max

Switching

7.5W max

		Bay Trail - M	Bay Trail - I
VCORE	SVID	13A	
VNN	SVID	15A	
V1P35S	1.35V	1.3A	
V1P8A	1.8V	65mA	
V1P8S	1.8V	10mA	
V1P5S	1.8V	N/A	
V3P3A	3.3V	50mA	
V3P3S	3.3V	33mA	
V1P0A	1.0V	325mA	
V1P0S	1.0V	2.75A	
V1P05S	1.05V	1.0A	
V1P2A	N/A	N/A	
V1P2S	1.2V	21.3mA	0 mA
VRTC	RTC	160uA	

Can be grounded if MIPI CSI not used.

Battery
3V

N-MOS

DDR3L 1066MHz (SDRAM x4)

+VDIMM	1.5A max
+VTT_DDR	0.5A max

0.27W*4 = 1.18W

+VTT_DDR:0.675V

LDO

1.8V

2.75A max

1.0A max

ALC282		
AVDD	5.0V	N/A
DVDD	3.3V	N/A
PVDD	1.8V	N/A

LAN RTL8111GS		
VDD3P3	3.3V	370 mA
VDD1P0	1.0V	300mA

eMMC		
VCC	3.3V	200mA
VCCQ	1.8V	150mA

CSI Connector	
3.3V	70mA

EXPANSION SLOT	
+3.3V_AUX	??A

FRONT USB3 * 1PCS	
5V	0.9A

FRONT USB2 * 1PCS	
5V	0.5A

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circuitco
Printed Circuit Board Solutions

1380 Presidential Dr Ste#100
Richardson, TX 75081

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MINNOWBOARD2 - POWER DELIVERY

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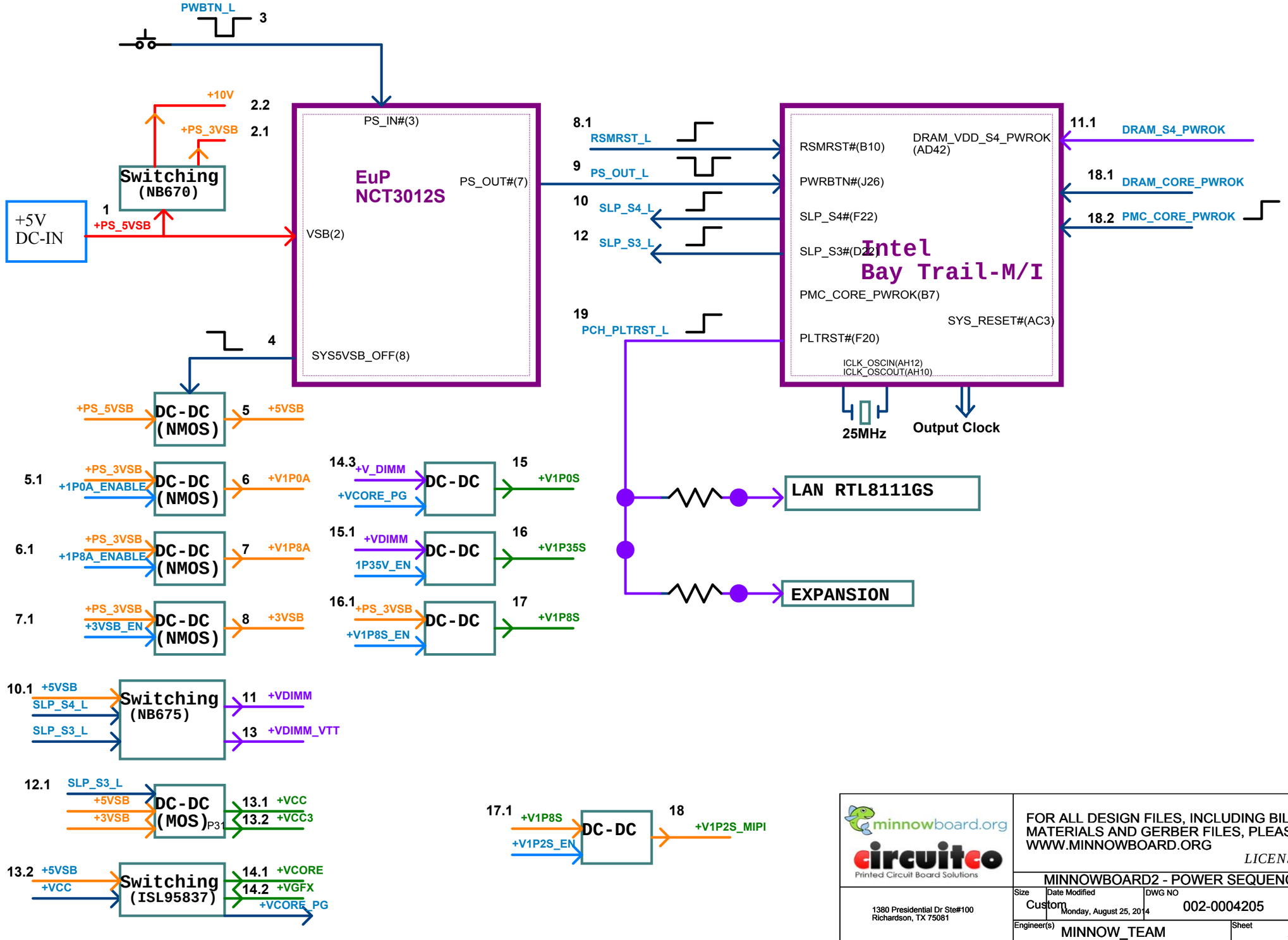
PWR Sequence & RST Diagram



MINNOWBOARD2 - POWER SEQUENCE

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